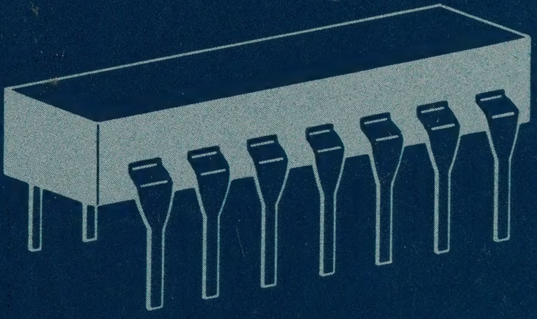
ELECTRONICS SERIES

Microelectronics: Devices and Applications



CHARLES BROOKS

Microelectronics: Devices and Applications

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PREFACE

This text is intended to provide a bridge from discrete component electronics theory, to linear integrated circuitry concepts, and to prelude the digital "chip." A wide sampling of linear IC concepts have been included to thoroughly acquaint the reader with a cross section of the numerous linear IC's available. The book is also intended to provide the theory necessary to apply these concepts to practical situations.

"Microelectronics: Devices and Applications," provides a source of some usually scarce information, such as an expanded explanation of Norton Amplifiers, while condensing some other topics, such as phase-locked loops, which have entire books dedicated to them. The overall objective is to initiate several diverse IC concepts at the discrete, or simple block diagram level, and develop them to the package level, instead of lightly explaining a large collection of linear IC's, as so many texts seem to do. In addition, the importance of the understanding and use of manufacturer's data sheets is stressed in each topic.

Ideally, this book is intended for the first time IC user. The reader should possess a basic knowledge of AC and DC electronics with transistor theory. It is written on a level for technicians and engineers engaged in the second year of a vocational school or community college electronics program. The book also provides a valuable source of information for the practicing technician or engineer, who finds that his knowledge of electronics has become somewhat outdated.

The topics included are presented in such a manner that an instructor can pick up the text and teach directly from it. Each topic is initiated in discrete form and developed through its package configuration. Also, many applications of the concepts discussed are included to reinforce the reader's understanding of the topics. Most topics are followed by a review, which utilizes a fill-in-the-blank type format. Each chapter ends with a summary of the chapter's highlights, to allow the reader to quickly refresh his knowledge of the chapter's contents. Included at the end of each chapter is a Chapter Progress Evaluation, to allow the student to test his understanding of the material. A glossary of terms is included as the final chapter.

INTRODUCTION

Microelectronics is the study of small, high density, compact electronic circuits. These circuits are composed of passive and active elements and their interconnections constructed on a single small semiconductor block, and are referred to as integrated circuits (IC). These circuits may contain from ten to tens-of-thousands of active and inactive components. IC's may be divided into two categories: monolithic and hybrid circuits. Monolithic circuits consist of entire functional circuits, constructed on a single block called a "chip." Hybrid circuits consist of two or more of these semiconductor blocks, interconnected to form a complete functional circuit.

Integrated circuits were introduced in the late 1950's and have truly caused a revolution in the electronics industry. The use of these tiny, prepackaged units has provided low cost, highly efficient compact circuitry for the industry.

Thousands of identical IC's are produced side-by-side in a single instant, which provides greatly reduced production costs. Since an entire circuit is produced on one small wafer of silicon, the number of circuit pieces and interconnections required for complex systems is greatly reduced, along with tremendous reductions in overall system sizes.

Integrated circuits can also be classified by the type of operation they perform. The two classifications of IC's are digital and linear circuits. Digital IC's are circuits designed to operate as on-off switches, and process information in the form of high and low voltage levels. These circuits are widely used in digital computers and process control logic circuitry. In this type of circuit, active elements are operated in two distinct states: cutoff or saturation. The high and low voltage states are used to represent the numbers of the binary number system (1 and 0) in logical operations. These chips may be composed of thousands of active and passive elements. An example of a digital quantity could be day and night. Except for short transition periods, (dusk and dawn), it is relatively easy to decide whether it is day or night. A classic example of a binary signal is the square wave. By randomly picking two instances of time, chances are those points will be at one of two values, +V or −V. If we disregard the square wave's transition times, we can assume the device is always at one of two values. These two values may be thought of in terms of off/on, true/false, yes/no, high/low, 1/0, and so forth.

This text is dedicated to the study of the linear integrated circuit families. These circuits are designed to generate or process analog signals. Most quantities are analog in nature, meaning they process an infinite number of possible values. A common sine wave is a classic example of an analog signal. Randomly picking any two points along the wave should produce two different levels of voltages. An analog signal may be defined as an AC or DC signal that varies smoothly and does not change abruptly.

Chapter 1 covers integrated circuit fabrication techniques and discrete operational amplifiers.

Chapter 2 uses the operational amplifier to introduce the reader to linear IC concepts and acquaint him with manufacturer's data sheets and IC terminology.

Chapter 3 provides a wide overview of common linear op amp circuit configurations and applications.

Chapter 4 looks at op amps and special IC's that are used to perform comparison operations, and some of the applications in which these comparators are used.

Chapter 5 covers op amp oscillators and function generators, which includes the 8038 IC function generator.

Chapter 6 compares passive and active filters and provides simple design procedures for higher-order filters.

Chapter 7 is dedicated to the concepts and applications of the Norton Amplifier.

Chapter 8 deals with a number of IC timers and their applications.

Chapter 9 develops a number of methods of providing regulated power supplies. These circuit concepts are developed in discrete form and finally covered in IC form.

Chapter 10 initiates the concept of the phase-locked loop and develops these concepts through the IC stage.

Chapter 11 covers a variety of selected special linear circuits and devices commonly encountered.

Chapter 12 provides a glossary of terms to help the reader in his studies of these circuits and concepts.

An appendix and glossary of terms are included to help the reader in his studies of these circuits and concepts.

In all honesty, the last thing I ever thought I would do was write a book. I would like to extend my thanks and appreciation to all of the people who made it work. To Teresa Arrington and Randy Ratliff for their abundant support, both moral and logistical. To Lisa Knotts, Judy Kee and Rachel Carson for their excellent typing skills. To Willie Amos, Chuck Hedrick, Jack Smith, and all of my fellow instructors for their invaluable help with this project. Special thanks to Paul Bock, for the use of his extensive electronics library and his consistent roll as devil's advocate on the way to and from work each day. Also to Morris Yates, for the use of his living room and fireplace where most of this material was prepared.

Lastly, thanks to Mike, Frank, and all the staff at National Education Corporation's Technical Publishing Division, for their help and interest in this project.

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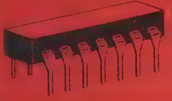


Chapter 1

Discrete Operational Amplifiers

Objectives

Upon completion of this chapter, you should be able to do the following:

- Describe the operation of common-emitter amplifiers
- List the basic stages of the operational amplifier
- Describe the operation of those basic stages

1-1 Introduction

Industrial electronics abounds with analog operations that have been crammed into linear IC's. Converters change frequency to voltage, and vice versa. Comparators test the relationship between two or more voltages. Timers set periods of operation or delay. Function generators and oscillators create signals that are both ordinary and unusual. Phase-locked loops keep signal frequencies within tight restrictions. In these, as in most other instances, an entire function has been contained inside one IC package.

All of these IC's incorporate one or more of the basic functions you will be studying, and some use old ideas in new ways. You'll spend the remainder of this chapter studying some important characteristics and applications of linear IC's.

1-2 IC Fabrication

Several kinds of processes are used in modern IC manufacturing. Let's begin by taking a look at some of the terms used to describe fabrication techniques, and the materials used in basic semiconductor structures:

Step grading
Linear grading
Grown junctions

Alloy junctions
Diffusion junctions
Epitaxial junctions

Words and phrases with broader implications are used to define the designs, materials, and treatments that go into complex semiconductor devices, in particular, IC's. Some examples are:

Substrate production
Epitaxial layers
Planar epitaxial growth
Masking and etching
Planar diffusion
Isolation diffusion
Lateral diffusion
Vertical diffusion
Double diffusion
Ion implantation
Dielectric isolation
Depletion-load NMOS (negative MOS)

Only a few differences separate linear and digital IC's when it comes to their manufacturing processes. The basic steps of fabrication are almost the same for both. **The fact is, the words *linear* and *digital* essentially describe modes of operation, rather than structures.**

However, certain differences in device characteristics do occur. For example digital diodes and transistors must switch—and transfer—at rates much faster than the diodes and transistors in linear service. This rate difference requires some slight changes in IC materials, as well as in how they're brought together and treated. You should also keep in mind that refinements in IC fabrication affect the performance and operating parameters of both digital and linear IC's.

In an IC, the substrate (supporting material within which an integrated circuit is fabricated) is either *P* or *N* material. In most constructions, one purpose of the substrate is to isolate the IC devices, such as transistors, diodes, and resistances, from each other. Thus, a *P* substrate contains NPN bipolar and *N*-channel FET devices, while PNP bipolars and *P*-channel FET's are found in *N* substrates.

Substrate crystals are grown (or drawn) as rods from molten silicon. Controlled amounts of impurities join the silicon as it is withdrawn from the melting pot. Injected boron turns the silicon into *P* material, with holes dominant. Phosphorus added to the silicon makes *N* material, with electrons dominant. For certain devices, extra doping creates *N*+ or *P*+ substrates.

Once grown and cooled, substrate rods are sliced into wafers approximately

0.006 in. (inches) thick. This about equals 150 μm (micrometers, or millionths of a meter, some times also called *microns*). Each wafer ranges in diameter from about 6 mm (millimeters), which is less than $\frac{1}{4}$ in., to 100 mm (about 4 in.) or more. One large wafer may be able to hold several thousand finished IC transistors and diodes.

Measurements of *resistivity* for a given cross-section determine proper doping concentration. If the substrate wafers pass this test, they're ready to receive the devices that turn them into IC's.

Not all IC structures use the substrate as an isolation material. Some processes, as a first step, grow a thin epitaxial layer onto the substrate, creating the opposite material. This process is referred to as epitaxial diffusion. **Figure 1-1a** illustrates an *N*-type epitaxial layer on a *P* substrate. This epitaxial layer is usually no more than 10 to 20 μm (0.01 to 0.02 mm) thick.

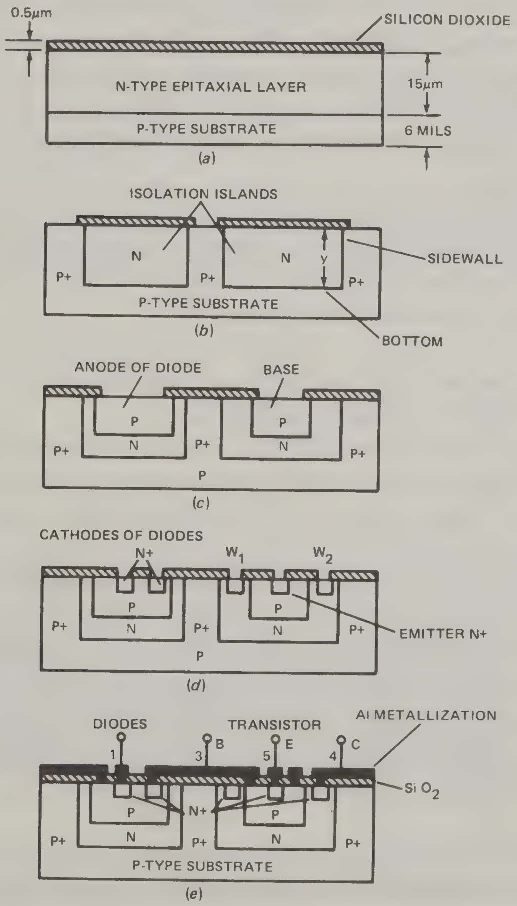

0.5μm
SILICON DIOXIDE
N-TYPE EPITAXIAL LAYER
15μm
P-TYPE SUBSTRATE
6 MILS
(a)
ISOLATION ISLANDS
N
N
y
SIDEWALL
P+
P+
P+
P-TYPE SUBSTRATE
(b)
BOTTOM
ANODE OF DIODE
BASE
P
P
N
N
P+
P+
P+
P
(c)
CATHODES OF DIODES
N+
W1
W2
P
P
N
N
P+
P+
P+
EMITTER N+
P
(d)
DIODES
TRANSISTOR
Al METALLIZATION
1
3
B
5
E
4
C
Si O2
P
N+
P
N
N
P+
P+
P+
P-TYPE SUBSTRATE
(e)

Figure 1-1. Making a transistor using epitaxial diffusion

In a second step, the epitaxial layer is given a steam bath at 1000°C (about 1750°F). Its surface oxidizes, forming a layer of silica, or silicon dioxide (SiO_2), about 0.5 μm thick. The silica forms an insulating layer, also shown in **Figure 1-1a.**

Next, the SiO_2 is coated with a *photoresist*, which is selectively exposed, through a mask, to ultraviolet rays. The exposed portions are then etched away, including parts of the SiO_2 layer, by acid baths. This masking and etching process, called *photolithography*, leaves a pattern of openings in the SiO_2.

High-temperature *diffusion* forces a heavy concentration of boron or other *P* dopant through the opening. This converts the uninsulated portions of the epitaxial layer into *P+* material. Unaffected areas become *isolation islands,* or *isolation wells*, of *N* material, as shown in **Figure 1-1b.**

Another steam bath deposits a new SiO_2 layer over everything. New openings are etched, again by photolithography. This time, diffusion forms *P* material inside the isolation islands, as shown in **Figure 1-1c**. These become the base elements for NPN transistors, or else form the *P* side of PN diode junctions.

Steam re-oxidizing, new photolithography, and more diffusion form *N+* blocks, as in **Figure 1-1d**. Some *N+* blocks are in the *P* bases and some in the *N* wells. These *N+* concentrations become *contact* blocks for the transistor collectors and emitters, or for diode terminals.

In a final step, this process vaporizes aluminum through a *metallization* mask. A selectively deposited aluminum layer provides interconnects and crossovers among the devices. The final result appears in **Figure 1-1e**, which illustrates one tiny section of wafer that's been processed this way.

Sometimes the term *planar* is used in connection with one type of epitaxial diffusion process, because it takes place on one side of a flat substrate wafer. One company calls its similar process *Isoplanar.*

Another process skips the step that forms the epitaxial layer. Instead, *N+* isolation islands are diffused directly into *P*-substrate material through openings etched in the silicon dioxide. From there on, this method, called *isolation diffusion*, or sometimes *double diffusion*, proceeds the same as with epitaxial diffusions.

A type of fabrication called *dielectric isolation* creates walls of nonconductive (or high-resistivity) material around devices. Silicon dioxide and silicon monoxide (SiO) are popular nonconductors. Aluminum oxides, in particular AL_2O_3, which includes the gems ruby and sapphire, are used occasionally. For silicon-on-sapphire (SOS) structures, an epitaxially grown layer of *N* silicon is etched away selectively, leaving semiconductor islands separated by high-resistivity alumina (aluminum oxide, or AL_2O_3). Beryllia (beryllium oxide, or BeO) is also used as an IC dielectric, but only rarely.

NPN is the favored bipolar junction transistor (BJT) structure in IC's. However, PNP transistors must sometimes be formed too, especially in linear IC's. A *lateral-diffusion* technique omits the final *N+* diffusion. Instead, two smaller *P* diffusions are substituted in place of what would otherwise be the base of an NPN device. **Figure 1-2** illustrates the PNP result.

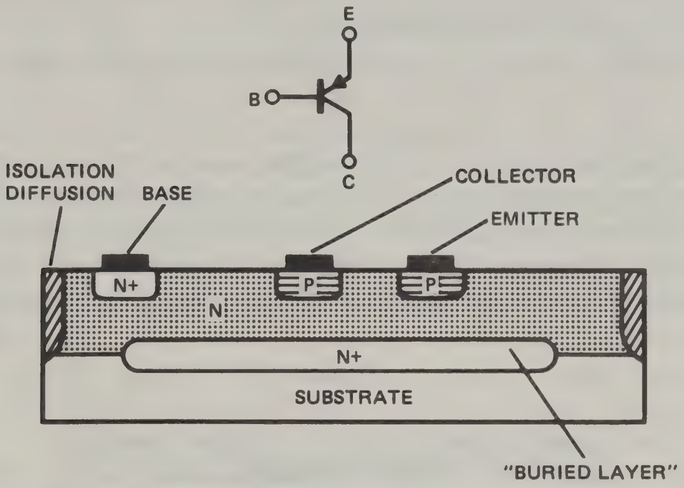

E
B
C
ISOLATION DIFFUSION
BASE
COLLECTOR
EMITTER
N+
P
P
N
N+
SUBSTRATE
"BURIED LAYER"

Figure 1-2. Latteral diffusion of PNP transistor into IC chip
Courtesy of Signetics Corporation

A *vertical diffusion* can also build a PNP transistor, as shown in **Figure 1-3**. The technique takes the substrate as the *P* collector, the epitaxial layer as the *N* base, and a *P*-base diffusion as an emitter. Contacts are deposited by special metallization.

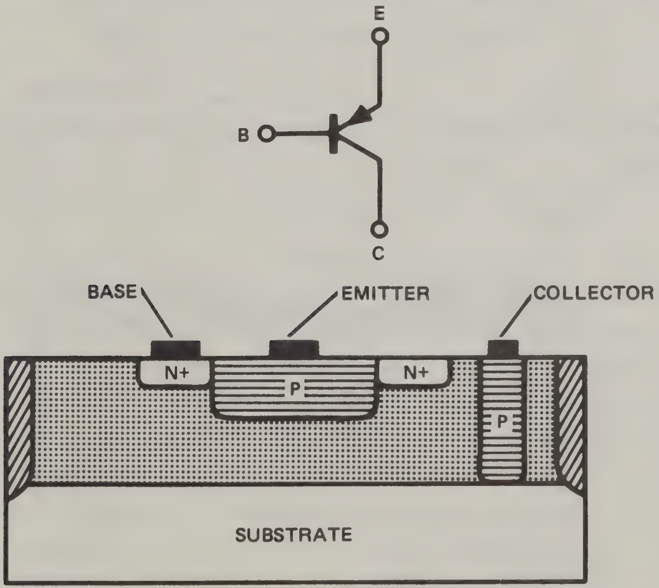

E
B
C
BASE
EMITTER
COLLECTOR
N+
P
N+
P
SUBSTRATE

Figure 1-3. Vertical diffusion of PNP transistor into IC chip
Courtesy of Signetics Corporation

Neither lateral nor vertical diffusions perform all that well, but thinning down the epitaxial layer can bring their parameters into usable ranges.

One matter, however, deserves elaboration: the differences between depletion- and enhancement-mode MOSFET structures.

Depletion MOSFET's, you may recall, behave much of the same way as JFET's. **An *N*-channel depletion MOSFET (called an NMOS) consists of a *P* substrate into which two *N*+ buttons and a lightly doped *N* channel have been diffused.** These form *drain* and *source* contacts, as shown in **Figure 1-4**. A layer of silicon dioxide masks everything but these contact points. Above the channel that forms between the drain and the source, the SiO_2 is very thin. An aluminum *gate* is deposited on this thin layer as other metallization is done. Negative voltage connected to this gate pushes *N* carriers away, depleting the majority (negative) carriers and pinching off current.

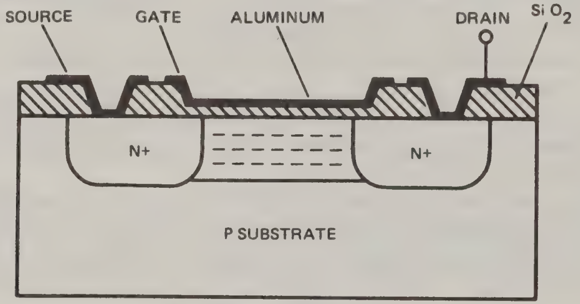


Figure 1-4. *N*-channel depletion MOSFET

With zero gate voltage (V_{GS}), or zero bias, the channel current, usually referred to as *drain current* and abbreviated I_D, depends on the drain-source voltage (V_{DS}) and channel resistivity.

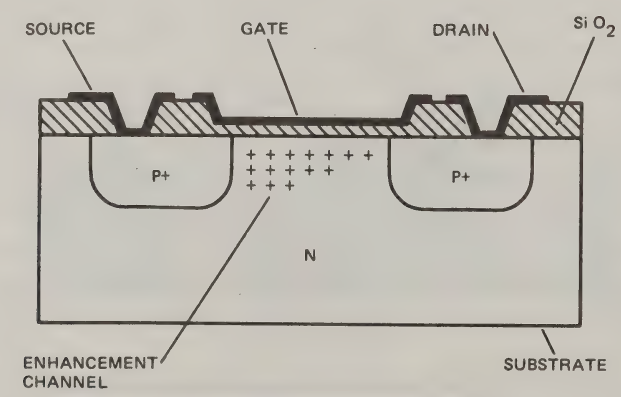
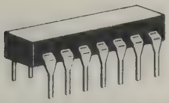


Figure 1-5. *P*-channel enhancement MOSFET



An enhancement MOSFET omits the channel diffusion. Otherwise, as **Figure 1-5** shows, it's physically similar to a depletion type. Its dimensions are smaller; however, distance from drain to source seldom exceeds 25μm, so the channel path is short. Diffusions are made shallow, only 2 or 3 μm deep, in an attempt to improve speed. Silicon dioxide and metallization are the same as for a depletion MOSFET.

The enhancement-mode structure in **Figure 1-5** is P channel. A substrate of N material contains two P buttons. With no diffusion between the drain and source, resistivity is high. Very little current flows, even with V_{DS} applied. However, a negative-bias voltage, V_{GS}, applied to the metal gate pushes negative carriers out of the way, creating a layer of positive carriers near the surface of the N material. This induced channel allows carriers (holes) to migrate freely between the P materials of source and drain.

With the advent of the LSI and VLSI (very large scale integration), standard photolithographic methods are no longer adequate. Computer-designed optical lenses have contributed significantly to better resolution for 1000 × (1000 times) reductions that have become common. Even so, in certain critical VLSI processes, lenses can't, without distortion, reduce masks to the submicroscopic dimensions needed.

Much work has been done with a new technique called *electron lithography*. Instead of photons or ultraviolet rays bombarding a photoresist, a beam of high-energy electrons strikes an electron-resist material. Ultimately, instead of the beam being directed through a mask, it can be deflected in modulated patterns, much like the beam in a televison picture tube. Etching is done by plasmas, mostly ionized gases, instead of by acid baths.

Few IC makers use such advanced technology, yet high-density, high-performance VLSI chips demand ever better techniques. Now we're into the exciting age of ULSI (ultra-large-scale integration), in which one chip holds millions of devices.

The matter of IC *speed* remains a challenge to IC designers. Considerable work on a new IC concept has been done toward the development of VHSIC (very high speed IC) devices. Today's fastest digital technology, the ECL family, tops out a little beyond 1 *GHz* (gigahertz, or 1 billion hertz). Goals for VHSIC include switching rates reaching to or even beyond 1 *THz* (terahertz, or 1 trillion hertz). The target is fifth generation computers and controllers, capable of performing a billion or more complex functions per second!

1-3 Packaging of IC's

Manufacturers seal IC's into their packages, a process called *encapsulating*, under tightly controlled conditions. Any substances left inside a sealed device contaminate it, either adding unwanted noise to the final product or shortening the life of the device.

A baking process, under vacuum, eliminates any water vapor that might later condense and oxidize metal runs and wire bonds, or cause leakage between circuit points. Final encapsulation may be done in a dry-nitrogen pressure chamber. (Nitrogen absorbs moisture.) There are several forms of encapsulation for modern IC's.

By definition, *hermetic sealing* means closing a device so tightly that no air can get inside. However, as used in today's IC technology, the term has a slightly different connotation. It still means airtight, but *all* IC's must be airtight, no matter what the sealing process.

Many modern IC's are packaged by *plastic molding*, generally the least costly of today's packaging processes. An insulating epoxy or plastic is molded around the chip, enclosing it and the bonding wires that connect device contacts (pads) to the external pins. There's no seam in plastic cases, since the entire case is molded right around the chip and its wires. **Figure 1-6** shows some plastic molded IC's.

Molded packages may be formed from one of several silicone or epoxy plastics. One popular new compound is *Epoxy B*, which also appears under the brand name *Epoxy Novolac*. Its inert composition reacts very little with the materials used in chip fabrication.

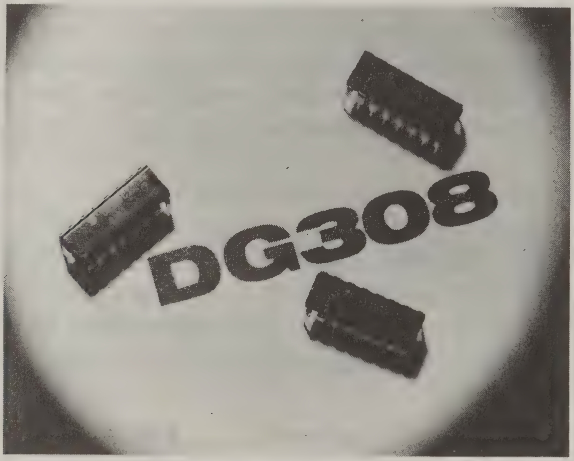


Figure 1-6. Encapsulating IC's using plastic molding
Courtesy of Siliconix, Inc.

Some molding is done with *ceramic* compounds. Ceramics are nonmetallic and are formed at high temperatures, well above the melting temperature of plastics.

Ceramic cases withstand higher operating temperatures than plastic molded types can.

Glass beads (called *frit seals*) may surround the leads where they pass through a molded ceramic case. The glass used has a low melting point, and therefore doesn't expand and contract as much as would a harder glass or ceramic. **This use of frit seals reduces stress on bonding wires whenever temperatures fluctuate.** Dual-in-line packages (DIP's) with this construction are called *Cerdip* types. Similar flatpacks are offered under the designation *Cerpak.*

Molded cases fill in tightly around the chip, the metallization, and the bonding wires. In contrast, the packaging for hermetically sealed IC's often leaves space, as you can see in **Figure 1-7**. This forms what is called a *cavity-type* package. The chip is first imbedded in an insulating body, usually of ceramic, beryllia (*BeO*), alumina (AL_2O_3), or glass. A lid, sometimes nickel or tin; sometimes glass or ceramic, completes the "compartment." Lids are welded into place as glass-to-glass, glass-to-metal, or metal-to-metal, to assure a seal.

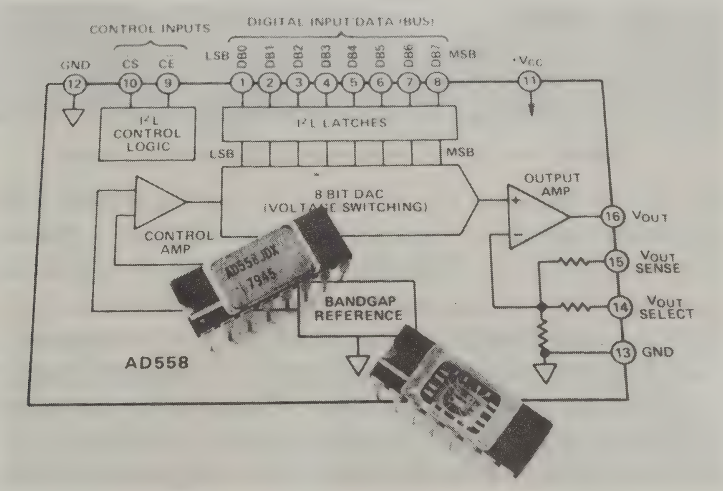

CONTROL INPUTS
DIGITAL INPUT DATA (BUS)
GND
CS
CE
LSB
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
MSB
+Vcc
12
10
9
1
2
3
4
5
6
7
8
11
I²L CONTROL LOGIC
I²L LATCHES
LSB
MSB
8 BIT DAC (VOLTAGE SWITCHING)
OUTPUT AMP
CONTROL AMP
16
VOUT
15
VOUT SENSE
14
VOUT SELECT
13
GND
BANDGAP REFERENCE
AD558
AD558JDX
7945

Figure 1-7. Hermetically sealed IC's
Courtesy of Analog Devices

A few metal packages are formed from two shells, into which the chip and insulating body are placed. The resulting package is called *side-brazed*, from the location of the brazed (welded) seam. The seal is, of course, hermetic.

Hermetic packaging has been abandoned for most small digital and linear IC's intended for commercial and industrial applications. Some plastics deteriorate under high temperatures, spreading their own contaminants over the surfaces and wiring inside an IC. However, new plastics developed for molding, such as *Epoxy B*, have overcome the problems of earlier molding materials.

Military specifications call for hermetically sealed packages, — whether of metal or of ceramic. The IBM computer card, pictured in **Figure 1-8**, shows IC's of this type, with metal cases. Also, makers of hybrid IC's still use hermetic sealing fairly extensively.

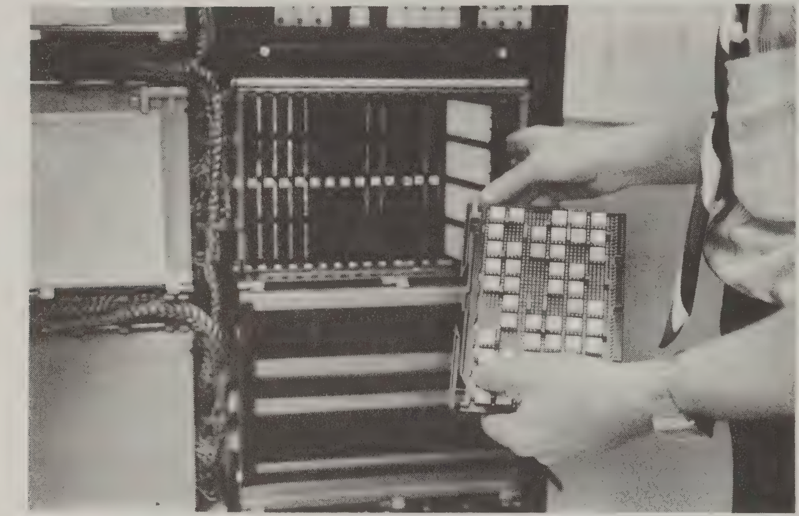


Figure 1-8. Hermetically sealed IC's with metal cases

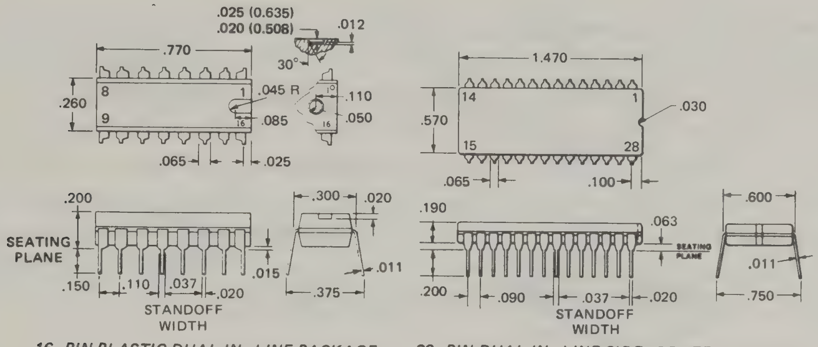
Every molding material has its advantages, but tests show fewer failures with epoxy than with plastic. (Both withstand vibration better than hermetic packaging.) However, extreme temperature fluctuations tend to break the bonding wires inside molded packages more so than in hermetically sealed devices.

After fabrication and encapsulation, most IC makers expose their products to stringent testing. For example, one manufacturer (National Semiconductor) bakes molded IC's for six hours at 150°C; puts them through five temperature cycles from 0°C to 100°C; tests operation at 100°C; and then, after the IC's cool to room temperature, runs them for a period of time at maximum voltage and current limits.

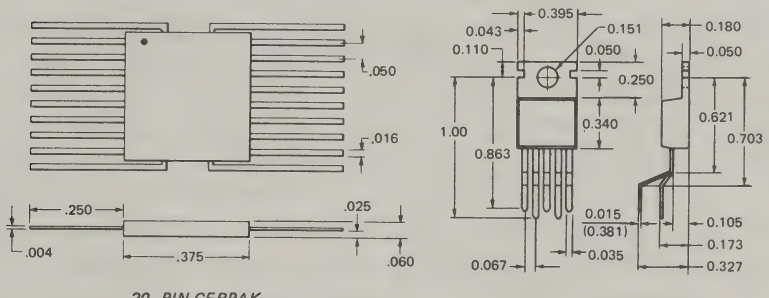
Other firms use similar stress procedures to weed out marginal IC's. Some tests are more demanding than that just described, others less so.

For military and other high-reliability applications, IC's must undergo a *burn-in* period after the tests described above. Burn-in involves operating the devices at maximum ratings, including the top military specification temperature of 125°C. Burn-in is then followed by a repetition of all the types of tests just described.

Some examples of standard *package outline* specifications appear in **Figure 1-9**. Labels and dimension drawings explain each of the outlines shown, and there are dozens of others. Data books include package outlines and dimensions, either on the specification pages for each device or in a section devoted entirely to outlines.


.025 (0.635)
.020 (0.508)
.012
.770
30°
.260
8
1
9
16
.045 R
.110
.085
.050
.065
.025
.200
.300
.020
SEATING PLANE
.015
.011
.150
.110
.037
.020
.375
STANDOFF WIDTH
1.470
.030
.570
14
1
15
28
.065
.100
.190
.063
.600
SEATING PLANE
.011
.200
.090
.037
.020
.750
STANDOFF WIDTH

16–PIN PLASTIC DUAL IN–LINE PACKAGE   *28–PIN DUAL IN–LINE SIDE–BRAZED PACKAGE*


.050
.016
.250
.025
.004
.375
.060
0.395
0.043
0.151
0.180
0.110
0.050
0.050
0.250
0.621
1.00
0.340
0.703
0.863
0.015
(0.381)
0.105
0.173
0.035
0.067
0.327

20–PIN CERPAK   *5–LEAD TO–220 POWER PACKAGE*

Notes
Leads are tin-plated alloy.
Base is AL_2O_3.
Cavity size is 200 x 300.

Figure 1-9. Examples of standard package outline specifications
Courtesy of Fairchild Semiconductors and National Semiconductor

One new kind of package is called a *leadless chip carrier*, or LCC. The carrier is square, with a cavity for the chip and its base, as illustated in **Figure 1-10**. A seal ring goes around the cavity. Instead of wires bonded to the contacts which must be "pinned out," metallic pads are used. These pads run from the chip cavity to the outer edge of the carrier. A lid goes over the cavity, hermetically sealed by side or edge brazing.

Eliminating conventional pins trims lead length in an LCC, and reduces capacitance between leads. The carrier can be very small, since its size depends more on chip dimensions than on the number of pinouts necessary. Connection pads are shorter than bonding wires in a DIP, and are spread more evenly around the package. Wider contact pads improve both current ratings and aid power dissipation.

This leadless package has been used more frequently in high-density hybrid devices than alone, and has opened new avenues in the miniaturization of small systems.

Three kinds of fields can affect IC's in an industrial environment (aside from heat, radiation or temperature). These are electric, magnetic, and radiological fields.

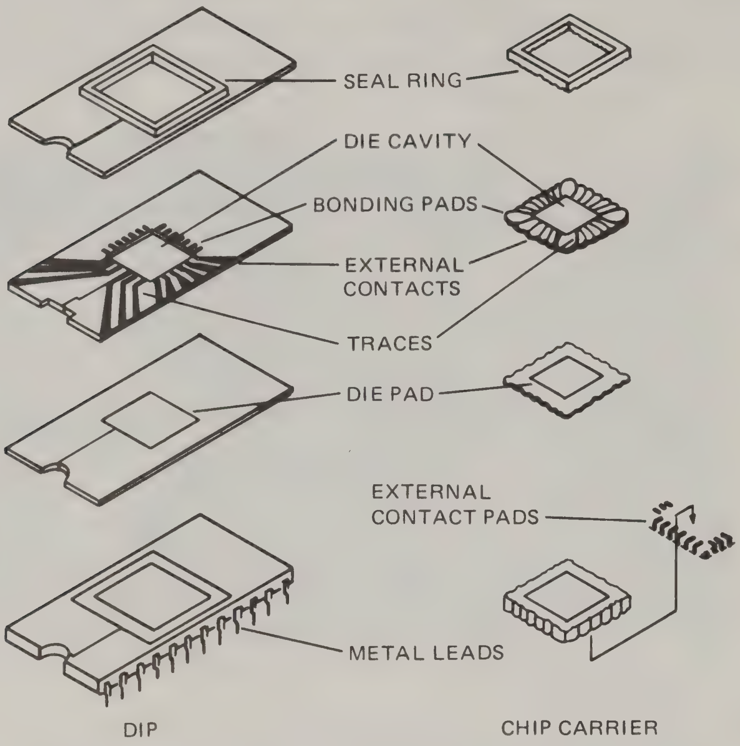


Figure 1-10. Hermetically sealed IC's with metal cases
Courtesy of Harris Semiconductor Products Division

Metal packaging, with hermetic seals, is often chosen for industrial environments, since this kind of construction helps shield out radiation of all kinds. Certainly, this kind of packaging is necessary in equipment for outer space, where all sorts of radiation are present.

Electric fields that affect IC's consist mainly of *electric noise*, in the sense that *noise* signifies unwanted signals. Electric noise comes from motors, generators, and RF (radio-frequency) equipment. Unsuppressed, such electric noise can swamp ordinary TTL, ECL, and small-signal linear devices. You therefore generally try to reduce electric noise at its source.

Certain random noise signals are hard to pin down, and sometimes even tougher to cure. They can be more destructive than ordinary industrial electric noise. Examples include the noise generated by static discharges in the vicinity of sensitive digital or linear circuitry; and the noise, similar to static noise, created by unlike metals rubbing together.

Modern IC's, especially sensitive CMOS (complementary MOS) devices, have some input-circuit protection built in. Others must be placed in shielded cages. **Copper and aluminum screen rooms or cages, if properly grounded, block most forms of radiated electric noise, whatever the source. Noise traveling over power lines, however, requires special filtering.**

Magnetic fields can noticeably affect IC operation, due to unwanted Hall effect. Mu-metal (a metallic alloy) shields and steel or iron plating ward off magnetic fields. However, the effectiveness of these shields and plating depends on how intense the field is. If possible, keep IC's and magnetic fields (such as from motors) well separated.

Radiological radiation is the toughest type of radiation from which to shield IC's. High-energy ray bombardment; mainly by cosmic, gamma, and X-rays, and by neutrons, can create several undesirable effects in IC structures. No practical IC packaging can block out these radiations, but specially shielded equipment cabinets can head off some of them. X-rays can be halted fairly well by lead (*Pb*) shielding, while boron (*B*) added to the lead deters certain gamma-ray activity. System components in radiation enviroments need to be housed in such cabinets.

IC's in molded packages show far less susceptibility to vibration damage than hermetically sealed IC's. The plastic or epoxy material fits tightly around bonding wires and contact pads, holding leads firmly.

In packages with cavities, leads depend mostly on their own strength and stiffness. Internal opens caused by vibration occur more often than with molded IC's. Some hermetically sealed packages contain insulation filler blocks that help. In others, body design supports the bonding wires, reducing strain on them.

1-4 IC Numbering Systems

Some IC's have a manufacturer identification stamped on the case, usually some kind of stylized trademark. All IC's show type numbers, and those for digital IC's have become rather standardized. They offer at least four, and usually five, items of information that help with identification. (Data books and specification sheets list IC's by these numbers.) They include:

1. Manufacturer product prefix letters (sometimes omitted).
2. Series, or family, identifier numerals.
3. Letter or letters indicating a subfamily (if the chip belongs to one).
4. Device identification number.
5. Letter suffix, usually relating to packaging, temperature rating, or both.

The five items in the two identification numbers below are separated at the right:

CD4032B	CD 40 XX 32 B
SN74ALS109J	SN 74 ALS 109 J

Here's what they mean:

CD = RCA digital
40 = CMOS family, if RCA (TTL, if Motorola)
XX = No subfamily given
32 = Triple serial adder
B = RCA high-voltage CMOS

SN = Texas Instruments bipolar
74 = TTL family
ALS = Advanced low-power Schottky subfamily
109 = Dual JK positive-edge triggered flip-flop
J = Motorola ceramic (high-temperature) package

Table 1 lists product abbreviations for several well-known manufacturers of both linear and digital IC's. **Keep in mind that a second-source manufacturer generally imprints the product prefix of the company that originated the design, relying on a *trademark* to indicate who actually made the IC.**

TABLE 1

Manufacturer/Product Prefixes for Linear and Digital ICs

Prefixes	Originating Company or Organization
AD	Analog Devices, Inc.
CA, CD	RCA Solid State Division
DM, DS	National Semiconductor Corporation
HA, HC, HD, HI, HM	Harris Semiconductor Products Division
JB, JM, M	Military
LF, LH, LM, LS	National Semiconductor Corporation
MC	Motorola Semiconductor Products Inc.
NE, SA, SD, SE, SG, SU	Signetics Corporation
SN, TA, TL, TS, TSM	Texas Instruments Incorporated
Si	Siliconix Incorporated
UA	Fairchild Semiconductors

Table 2 lists a few IC family designators, most of which are still in use. However it's by no means a complete listing.

You're already familiar with most digital TTL subfamily lettering, but it's gathered together in **Table 3.**

TABLE 2

Designators for IC Families

Family Numbers	Company and Family	
12, 16	Motorola	ECL
30, 31	Motorola	TTL
32–38	Fairchild	MOS
40, 44, 45	RCA	CMOS
40, 43	Motorola	TTL
43	Texas Instruments	CMOS
54 (C)	National Semiconductor	CMOS
54	Texas Instruments	TTL
70–72	National Semiconductor	TTL
74 (C)	National Semiconductor	CMOS
74	Texas Instruments	TTL
75	Texas Instruments	Interface
76–88	National Semiconductor	TTL
90–96	Fairchild	TTL
101–125	Motorola	ECL
140–145	Motorola	CMOS

TABLE 3

TTL Subfamily Letters

ALS = Advanced low-power Schottky
C = CMOS
F = Fast-advanced Schottky
H = High-speed
L = Low-power
LS = Low-power Schottky
S = Schottky

You'll find related device numbering. A 109, for example, generally contains the same digital or analog functions internally, even in several different brands, families, and subfamilies. However, be careful with this: **as newer families appear, device numbers are reused, and consequently will not always signify the same device in another family or from another IC maker. Always check the appropriate data book.**

Suffixes generally are unique to each manufacturer. They refer to package style, to packaging material, to temperature ratings, or to whatever else an IC maker decides to use them for. **In the front or back of most data books are charts explaining the meanings of the suffixes used in the book.**

Manufacturers place data for digital and linear IC's in separate books. Since there are so many kinds of IC's, you may find data books segregated even further, by product use or by family.

Some examples of data-book categories follow:

RCA Solid State Division:
  Linear IC's
  High-reliability IC's
  COS/MOS IC's
  COS/MOS memories, microprocessors, and support systems
  Power devices

Fairchild Semiconductors:
  Linear Division products
  Linear interface data book
  TTL data book
  FAST data book
  CMOS data book
  Bipolar memory data book
  MOS memory data book
  Optoelectronics data book

These represent only some of the data books available from just two companies. Other IC makers offer broad lines of IC products, and therefore publish many data books. An few examples are listed below:

Analog Devices, Inc.
Datel-Intersil, Inc.
Fairchild Semiconductors
Harris Semiconductor Products Division
Mostek Corporation
Motorola Semiconductor Products Inc.

RCA Solid State Division
Signetics Corporation
Siliconix Incorporated
Standard Microsystems Corporation
National Semiconductor Corporation
Precision Monolithics Incorporated
Texas Instruments Incorporated, Semiconductor Group

Some of their data books are illustrated in **Figure 1-11**.

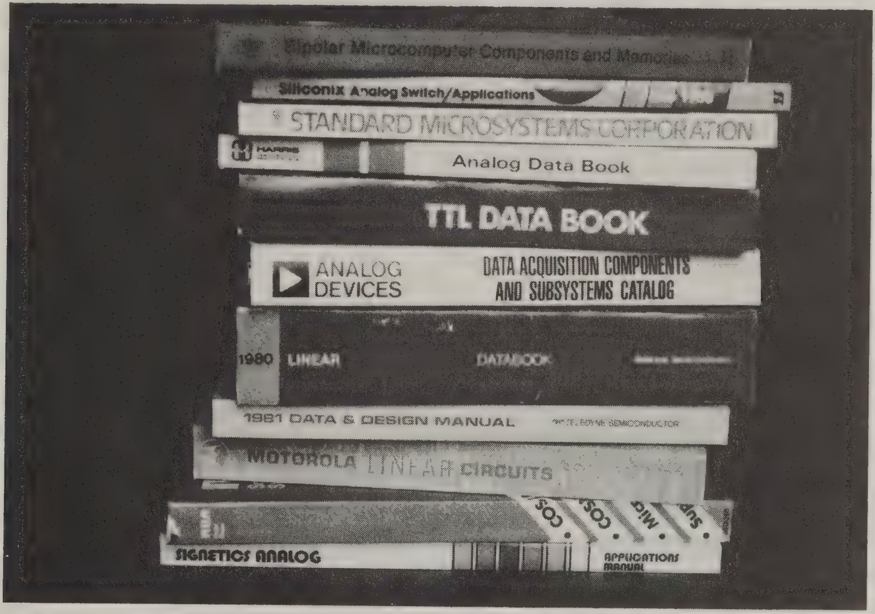

Bipolar Microcomputer Components and Memories
Siliconix Analog Switch/Applications
STANDARD MICROSYSTEMS CORPORATION
HARRIS
Analog Data Book
TTL DATA BOOK
ANALOG DEVICES
DATA ACQUISITION COMPONENTS AND SUBSYSTEMS CATALOG
1980 LINEAR DATABOOK
1981 DATA & DESIGN MANUAL
MOTOROLA LINEAR CIRCUITS
SIGNETICS ANALOG
APPLICATIONS MANUAL

Figure 1-11. Manufacturer's IC data books

Many other companies manufacture IC devices. Those shown are only some of the products available from some of the manufacturers.

Two kinds of applications lead to hybrid integrated devices: those demanding medium to high power, and those mixing digital with linear technologies.

Hybrid devices often have regular IC's inside, along with other components. Special encapsulation seals all components inside the package, which is itself generally larger than an ordinary IC. Pinouts may resemble those of digital and linear IC's you've seen already, though often the hybrids have more or heavier pins and larger outsize package dimensions. You can see one such hybrid package in **Figure 1-12**.

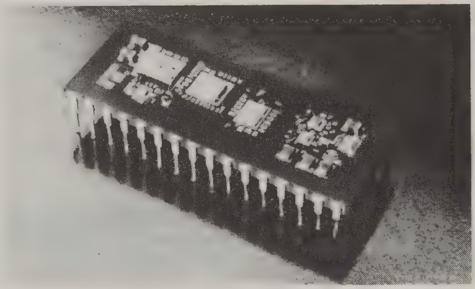


Figure 1-12. The leadless chip carrier
Courtesy of Analog Devices, Inc.

Hybrid devices function as:

Instrumentation amplifiers
Isolation amplifiers
Logarithmic amplifiers
AC (alternating current) to DC (direct current) power supplies
Industrial transducers
Signal conditioners
Digital-to-analog converters
Analog-to-digital converters
Frequency-to-voltage converters
Voltage-to-frequency converters
Sample-hold amplifiers
Track-and-hold amplifiers
Synchro-digital converters
Subsystems for data acquisition

Data books are available for hybrid devices too. Some titles:

Data Acquisition Components and Subsystems (from Analog Devices)
Data Acquisition Component Handbook (Datel-Intersil)
MC14500B Industrial Control Unit Handbook (Motorola Semiconductor Products)
Analog Data Book (Harris Semiconductor Division)

Some linear and digital IC data books can be obtained free, or at a nominal charge, from IC manufacturers' representatives and distributors. You may have to pay more for hybrid data books. Those that are worth their price describe theory and applications of the devices, besides specifications and operating data. Hybrid devices contain more than just simple transistors, resistors, and diodes, and most users need the extra information and suggestions.

1-5 Common-Emitter Transistor Operation

As an introduction to the operation of integrated circuits, discrete component operation of the bipolar transistor must first be discussed. Common-emitter circuit configurations are most often used in IC operation and are mentioned as a matter of review, since this particular configuration was covered in some detail in a previous text.

Bipolar transistors may be connected as shown in **Figure 1-13**.

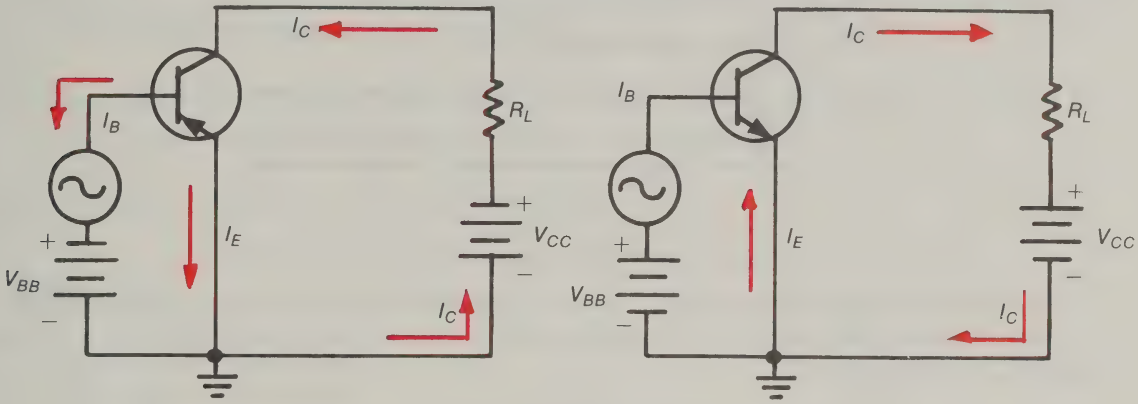


Figure 1-13. Common-emitter circuit configurations

The input signal is applied between the base and emitter of both NPN and PNP transistors, while the output is taken from between the collector and emitter of each. In these configurations, the emitter is common to both the input and output. It can be seen that the emitter-base junction of each transistor is forward biased, while the collector base junctions are reverse biased. This is an important characteristic of the common-emitter circuit configuration. It means that this particular circuit arrangement has a low input impedance, approximately 150 ohms, and a relatively high output impedance, in the neighborhood of 60,000 ohms.

The amount of current gain that a common-emitter transistor can provide can be determined by measuring the change in collector current for a particular change in base current, provided that V_{CE} is held constant. This current gain is represented by the Greek letter beta (β) and is expressed by the following equation.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

The current gain of a transistor is stated simply as a ratio with no specific unit of measurement assigned.

As an example of current gain in the common-emitter transistor, we will assume that V_{CE} remains constant at 10 volts and that I_B changes from 150 to 200 μA.

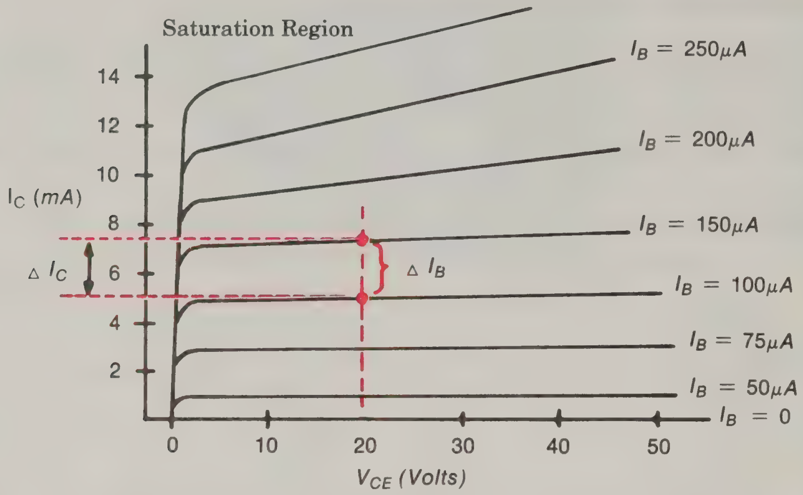


Figure 1-14. Typical transistor characteristic curves

Looking at **Figure 1-14**, we can see that increasing I_B by 50 μA *causes a change in* I_C of approximately 2.5 mA. Inserting these values into the equation for β, we obtain a current gain of:

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{25\ mA}{50\ \mu A} = 50$$

Our calculation shows that for the transistor represented in **Figure 1-14**, the current gain is 50, not uncommon for medium and low-power transistors.

Normally, manufacturers specify the minimum beta that a particular type of transistor has.

The beta just discussed is a measurement of the transistors AC current gain, since it is a ratio of a change in collector current to a change in base current.

Common-emitter amplifiers, because of their configuration, have voltage, current, and power gain. They also exhibit phase inversion of the input signal.

TYPE	VOLTAGE GAIN	CURRENT GAIN	INPUT/OUTPUT SIGNAL PHASE RELATION	INPUT IMPEDANCE	OUTPUT IMPEDANCE
COMMON-BASE	HIGH	<1	IN PHASE	LOW	REASONABLY HIGH
COMMON-EMITTER	HIGH	HIGH	180° OUT-OF-PHASE	REASONABLY HIGH	REASONABLY HIGH
COMMON-COLLECTOR	<1	REASONABLY HIGH	IN PHASE	REASONABLY HIGH	LOW

This previous review will be helpful in understanding linear IC circuit operation from a discrete point of view. Later, block diagrams and functional diagrams serve to give a better understanding of IC's, those both linear and digital in nature.

Topic Review 1-5

1. The characteristics of the common emitter amplifier are ______ ______ ______, ______ ______ ______, and ______ ______ ______ from input to output.

2. The gain of the common emitter amplifier, A_V, equals ______.

3. However, in dealing with signal currents that are amplified by the common emitter configuration, A_V will also equal ______.

4. The current gain of the common emitter amplifier is a measure of change in ______ current, divided by a change in ______ current.

5. This gain is termed ______ and is written β.

Answers

1. high input impedance
   low output impedance
   180° phase inversion
2. $\dfrac{V_{\text{out}}}{V_{\text{in}}}$
3. $\dfrac{R_C}{R_E}$
4. collector
   base
5. Beta

1-6 Constant-Voltage References

Constant-current sources are circuits designed to provide a constant level of current over a specified range of load variations.

The use of constant-voltage references in IC's also provides very high performance circuits, because any changes in operating temperature are compensated for on the chip itself. Constant voltage references also lend dependable operating parameters to the chip from application to application.

Manufacturers use several methods to produce constant voltage references. The most popular means of establishing these references are: the use of the voltage dropped across a forward biased diode junction, the reverse biased diode junction, and the breakdown voltage of the reverse biased zener diode.

The forward biased diode method is preferred over the reverse biased method, because the breakdown of the reverse biased method is never used in chips intended for low noise applications, and is never used directly in the signal path of the chip. Although the actual value of voltage dropped across the forward biased diode varies from chip to chip, it may be assumed to be constant at 0.6 volts. In reality, this level may be as low as 0.5 volts or as high as 0.7 volts.

Constant diode voltage drops may be used in a number of ways within the IC. A single diode junction may be used to control the biasing of a transistor or to "clamp" voltage levels within the chip. Series connected diode junctions may be used to establish higher levels of constant voltage. Some chips even use a special section of the wafer for a constant voltage reference section. **Figure 1-15** shows a stack of series connected diodes which are used to supply various levels of constant voltage to the rest of the chip.

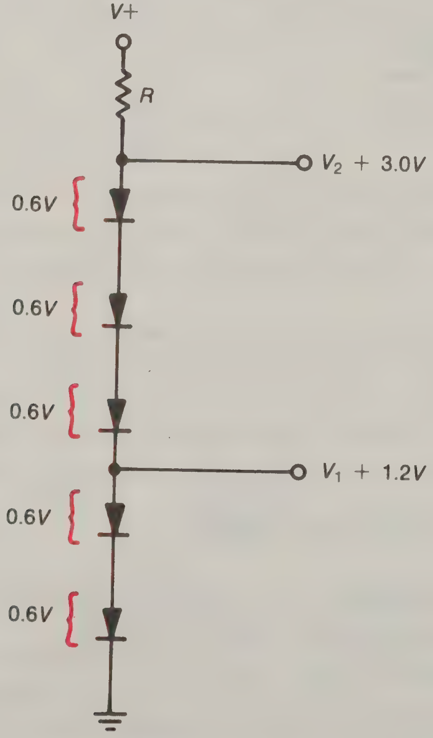


Figure 1-15. A constant-voltage diode stack

It is easier for manufacturers to produce an IC transistor than a diode junction. For this reason, the actual schematic of a chip shows a transistor with its base and collector shorted together as shown in **Figure 1-16a**. The only voltage dropped in this configuration is the 0.6 volts dropped across the base-emitter junction of the transistor.

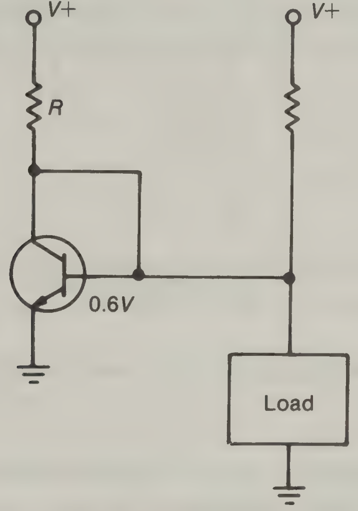


Figure 1-16a. An IC constant voltage diode

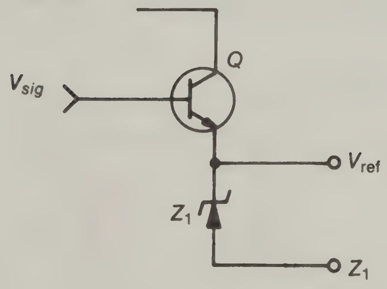


Figure 1-16b. A undedicated zener diode in an IC package

Reverse-biased zener diodes are also used to establish various levels of constant voltage. The manufacturer designs the zener diode circuitry to operate in the diode's avalanche region, which can be assumed to produce a constant level of voltage under changing signal and load conditions. Some IC chips include undedicated (not actually used by the chip) zener diodes on the chip to allow the user to extend the operational characteristics of the chip as shown in **Figure 1-16b**. In this configuration, the zener diode may be employed by the user to extend the level in which V_{sig} must reach in order to turn Q_1 on. Stated another way, the emitter of Q_1 is no longer at ground potential when the transistor is forward biased. Instead, the emitter is at some voltage above ground, depending on the breakdown voltage of Z_1. Therefore, V_{sig} must be that much more positive in order to turn Q_1 on. Undedicated zener diodes are also included in IC packages to allow the user to provide independent levels of reference current to the chip. This practice is not widely used because the inclusion of undedicated zener diodes requires that extra pins be added to the package, increasing the cost of the IC.

Topic Review 1-6

1. One of three most popular methods of producing constant voltage references in IC's is the use of the voltage dropped across a ________ ________ diode junction.
2. One method used to establish higher levels of constant voltage is to connect the diode junctions in ________ .
3. Since it is easier for IC manufacturers to produce transistors instead of diodes, the actual schematic of an IC chip will show the ________ and ________ of the transistor shorted to each other.
4. Reversed-biased ________ ________ are also used to establish various levels of constant voltage.

Answers:

1. forward-biased
2. series
3. base
   collector
4. zener diodes

1-7 Constant-Current Sources

Constant-current sources are circuits designed to provide a constant level of current over a specified range of load variations.

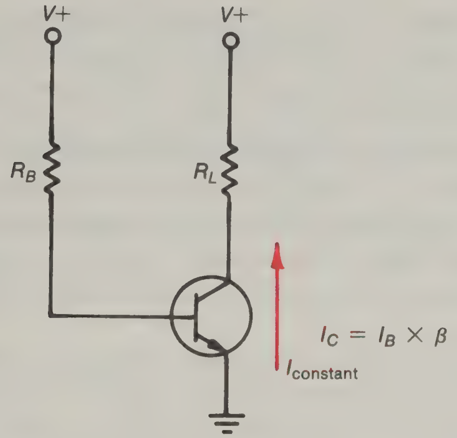


Figure 1-17. A simple constant current source (large amounts of base resistance required).

As shown in **Figure 1-17**, this circuit depends on large values of base resistance (R_B), and the value of transistor current gain (β) to determine the level of constant current. This arrangement also has very poor temperature stability because of the different temperature characteristics of the resistance material and the transistor materials. Also remember that resistors basically transform electrical energy to heat. The range of loads to which the circuit can provide a reasonably constant amount of current is severely limited. All of these limitations are inappropriate for IC design, so designers have developed better methods for providing constant current.

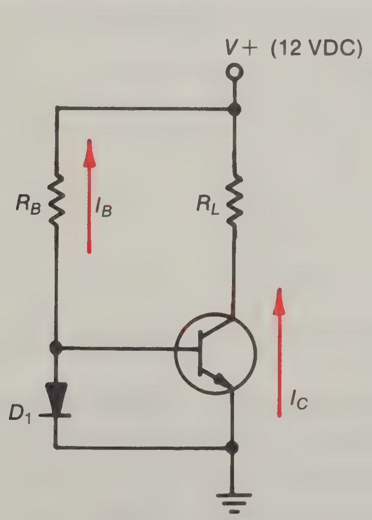


Figure 1-18. An improved constant current source.

As shown in **Figure 1-18**, the forward biased diode junction (D_1) maintains a constant level of voltage (0.5 to 0.7 volts) on the base of the transistor. Resistor R_B simply limits the current through the diode and has to drop approximately 11.4 volts.

With the base voltage clamped at 0.6 volts, I_C is approximately equal to and dependent on I_B. Since the diode junction and the base-emitter junction are made of the same materials, the voltage drops across them are nearly identical and changes in temperature should effect both equally. I_C is now much closer to being constant over a fairly wide range of values of R_L. Load current can be controlled further by this configuration.

As shown in **Figure 1-19a**, if the load changes, calling for more current, resistor R_E senses the current increase and drops more voltage, reducing the forward bias on the base-emitter junction of the transistor. This in turn, reduces the base current, reducing the increase in collector current. In other words, the presence of R_E compensates for the β of the transistor to keep I_C constant. It is important to realize that this process is very automatic.

If R_E is replaced by a variable resistance sensing element such as a thermistor, the constant current source can be converted to a 4 to 20 mA current transmitter for instrumentation applications.

As a practical example, let's say your boss comes to you and wants you to design a 1 mA constant current source. Where do you start?

The general form is known, the value of constant current is known, and the level of base voltage is known.

$$I_C = 1\ mA \text{ (desired)}$$
$$V_B = 1.2 \text{ VDC (clamped by the diodes)}$$

The first thing to find is a value of resistance for R_E. The base-emitter junction of the transistor drops about 0.6 volts. That leaves 0.6 volts to be dropped across the emitter resistor. Remember that for all practical purposes, I_E equals I_C.

$$\text{next:} \qquad R_E = \frac{0.6\ V}{1\ mA}$$

$$\text{then:} \qquad R_E = 600\ \Omega$$

The last detail to be considered is the maximum load to which the current source can supply constant current.

For proper operation, the transistor's collector voltage must not drop lower than the base voltage to maintain the reverse bias on the base-collector junction.

The collector voltage is the same as the base voltage when R_L drops 10.8 volts (12 volts $-$ 1.2 volts). Since I_C equals 1 mA, R_L drops 10.8 volts when it equals:

$$R_L = \frac{1.2\ V}{0.001\ A} = 1200\ \Omega$$

Provided R_L stays well below this value, this particular circuit will serve as a constant current source. Thus the circuit in **Figure 1-19a** can be replaced by the symbol in **Figure 1-19b**.

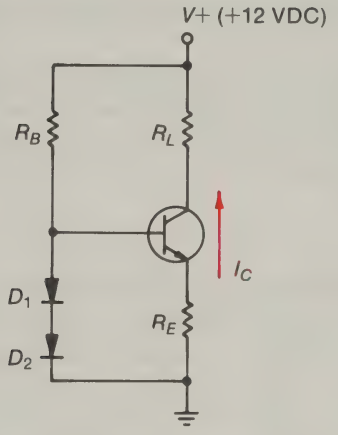


Figure 1-19a. A constant current source with better current control

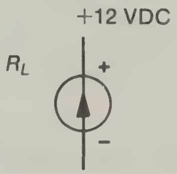


Figure 1-19b. A constant current source schematic symbol

As shown in **Figure 1-20**, by using a split power supply, the load handling capability of the current source will be greatly increased.

The voltage level of the transistor's base is now clamped at −10.8 volts (12 volts − 1.2 volts). The value of R_E remains the same as before, and the voltage on the

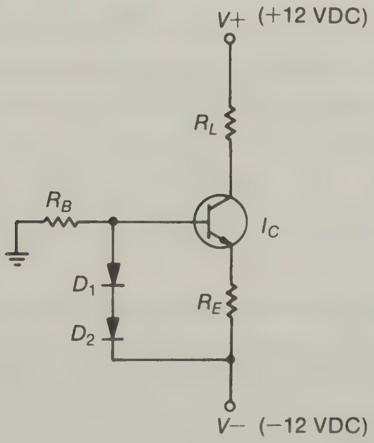


Figure 1-20. Constant current source with split voltage supplies for larger load handling capabilities.

emitter is now −11.4 volts. The voltage drop across R_L is now 12 volts minus −10.8 volts, or 22.8 volts. If I_C remains at 1 mA, then the maximum load resistance, R_C, can now be increased.

$$R_L = \frac{22.8\ V}{0.001\ A} = 22.8\ k\Omega$$

The value of maximum load has been increased greatly by incorporating a dual power supply.

In the monolithic fabrication process, it is easier to produce a constant voltage source by constructing an NPN transistor and shorting out the base-collector junction than it is to construct a diode junction. So, a constant current source in IC form takes on the general appearance shown in **Figure 1-21**.

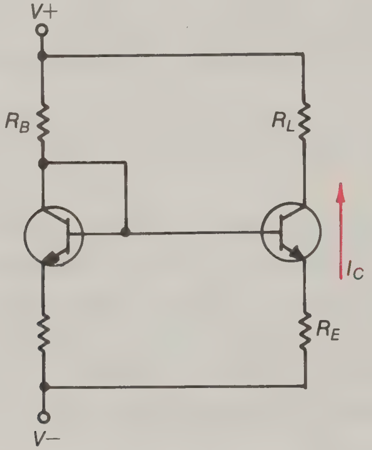


Figure 1-21. *IC* configuration of a constant current source.

Since all the components are produced by the same machine, on one substrate, and baked in the same oven, the components are extremely well matched. The base-emitter bias voltage of both transistors, and therefore the base currents, are very nearly identical. Values of resistance are very well proportioned and the overall achievement is a stable temperature, gain, and independent constant current source.

Another common practice in IC circuits is the use of constant current sources in series.

It is not practical to develop the small currents used in IC's from a single current source. Also, it was pointed out earlier that exact values of resistance, capacitance, and current gain cannot be achieved, but relative values of these quantities can be established with great accuracy. In the case of current, the use of series current sources allows very small constant currents (300 na) to be developed, as shown in **Figure 1-22**.

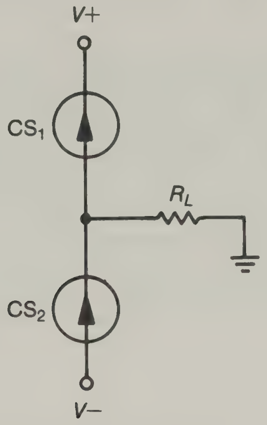


Figure 1-22. Series current sources.

The output current of series current sources is limited to the value of the smallest source. If CS$_1$ and CS$_2$ are equal, let's say to 1 *mA*, then 1 *mA* flows from $V-$ to $V+$. The current through R_L will be zero (Kirchhoff's current law: The sum of the currents entering a junction equal the sum of the currents leaving a junction).

If the current sources are not equal, the difference current flows through the load (R_L). See **Figure 1-23**.

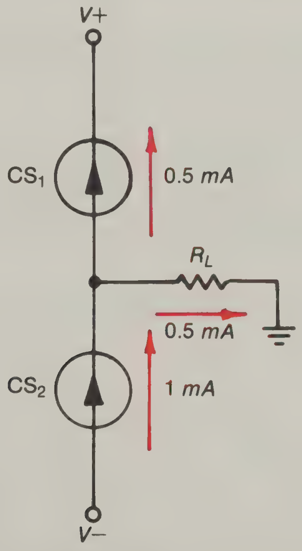


Figure 1-23. Unequal series current sources produce a difference current through the load.

The excellent control of relative values in IC's allows very small currents to be produced from series current sources. This is shown in **Figure 1-24**.

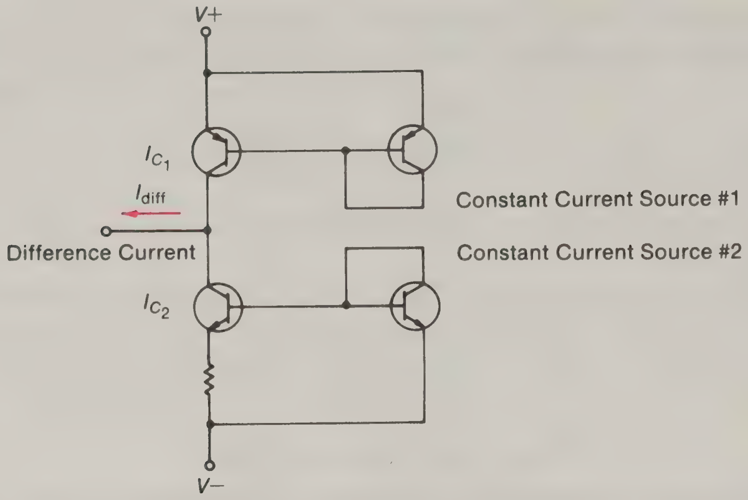

V+
I_{C_1}
I_{diff}
Difference Current
Constant Current Source #1
Constant Current Source #2
I_{C_2}
V−

Figure 1-24. IC series current sources

Topic Review 1-7

1. Constant current sources depend on large values of ______ resistance and the value of ______ to determine the level of constant current.

2. It can been seen from **Figure 1-19a** that the presence of ______ compensates for the ______ or ______ of the transistor to keep I_C constant.

3. The purpose of R_B in **Figure 1-19a** is to limit ______ to D_1 and D_2.

4. By using a ______ ______ ______, the load handling capability of the current source will be greatly increased.

5. A common practice of IC manufacturers is the use of constant current sources in ______.

Answers:

1. base
   beta
2. R_E
   gain, beta
3. current
4. split power supply
5. series

1-8 Differential Amplifiers

The differential amplifier is the basic building block of many integrated circuits. It was originally developed to respond to the difference between two input signals (analog computer math). Differential amplifiers are capable of both AC and DC amplification. They also provide superior noise rejection.

As shown in **Figure 1-25**, notice that the diff-amp is symmetrical in nature; it has two inputs,applied to the bases of transistors Q_1 and Q_2, and two outputs,taken from the collectors of Q_1 and Q_2. It is supplied by a constant current source and operates with a dual-voltage power supply ($V+$ and $V-$).

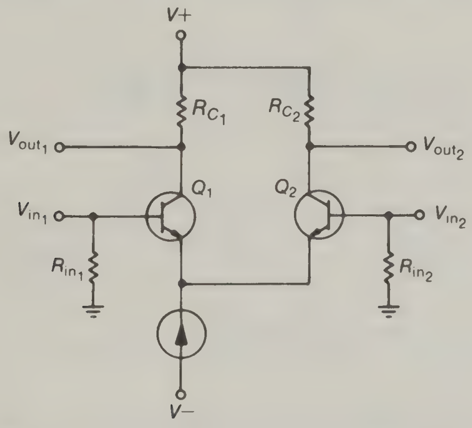


Figure 1-25. A simple differential amplifier

To operate properly, transistors Q_1 and Q_2 need to be very closely matched, as do resistors R_{C_1} and R_{C_2}. Integrated circuit fabrication techniques fulfill these requirements quite well, and also provide this circuit with excellent temperature stability.

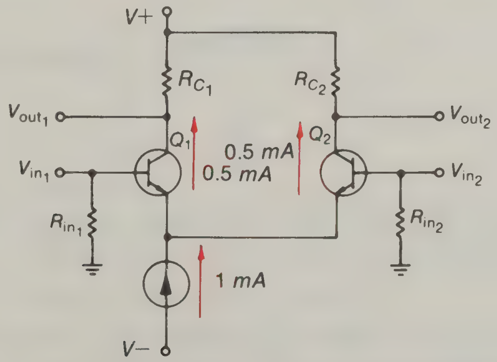
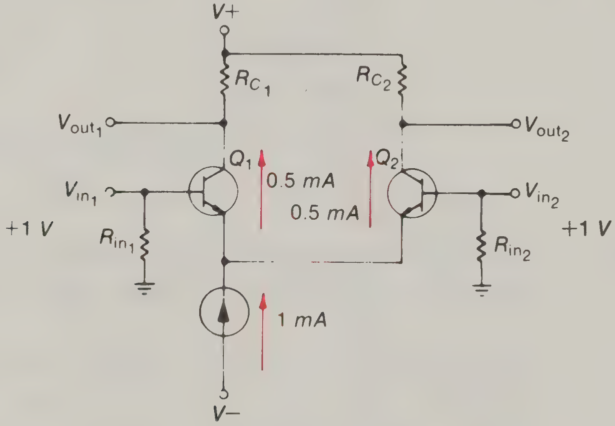


Figure 1-26. Differential amplifier with no input signal applied.

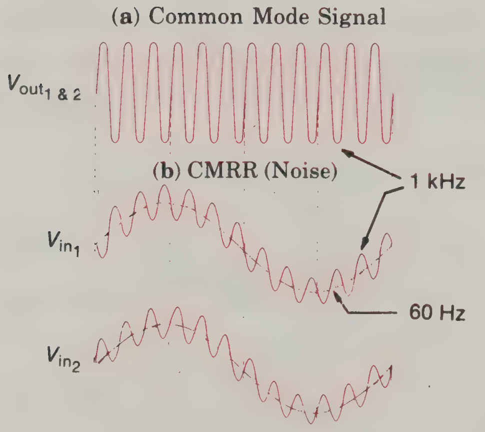
As shown in **Figure 1-26**, with no signal applied to input V_{in_1} or V_{in_2}, the current from the constant current source will be divided equally between the two identical branches of the amplifier. Therefore, V_{out_1} equals V_{out_2}.

$$V_{out_1} = V_{out_2} = V+ - (\tfrac{1}{2} I_{const} \times R_{C_1})$$

If identical $+1\,V$ signals are applied to transistors Q_1 and Q_2 as shown in **Figure 1-27**, each will try to conduct more current. Since the constant current source can only supply $1\,mA$, there cannot be an increase through the branches. When the current does not change, the output voltage remains the same. Hence, common input signals are rejected in the sense that the amplifier does not respond.



(a) Common Mode Signal



(b) CMRR (Noise)

Figure 1-27. A differential amplifier with equal input signals applied.

This ability to reject identical (common mode) input signals is an important feature of a differential pair. This provides an excellent means to reduce hum and noise.

Even with the excellent component matching done with IC technology, the components are not identically matched. One transistor may have slightly more gain than the other transistor, or the resistors may be an ohm or two different, and some common mode signal may make it through the differential amplifier to the output. However, the differential amplifier tends to reject a common mode signal and amplifies a differential signal. How well the differential amplifier performs this task is expressed as the amp's *common mode rejection ratio* (CMRR).

CMRR is a comparison between how well the amplifier amplifies a differential signal and how well it rejects a common-mode signal. This can be mathematically stated as follows:

$$\text{CMRR} = \frac{A_{vd}\,(\text{differential})}{A_{vcm}\,(\text{common-mode})}$$

because:

$$A_v \text{ differential gain} = \frac{V_{\text{out}}}{V_{\text{in}}} \quad \left(\begin{matrix}\text{differential}\\ \text{signal}\end{matrix}\right)$$

$$A_v \text{ common-mode gain} = \frac{V_{\text{out}}}{V_{\text{in}}} \quad \left(\begin{matrix}\text{common-mode}\\ \text{signal}\end{matrix}\right)$$

Let us say that a 0.1 volt differential input signal comes out of the differential amplifier at 10 volts, while a 0.1 volt common-mode input signal is reduced to 0.05 volts at the output. The CMRR would be as follows:

$$\text{differential gain} = \frac{10V}{.1V} = 100$$

$$\text{common-mode gain} = \frac{.05}{.1} = .5$$

$$\text{CMRR} = \frac{100}{.5} \text{ or } 200$$

The amplifier shows 200 times more gain for a differential signal than a common-mode signal. CMRR is usually expressed in decibels.

$$\text{CMRR}\,(dB) = 20 \log 200$$
$$\text{CMRR} = 46 \text{ dB}$$

It is common to have CMRR's of over 100.

This brings us to the question: How do we get the differential amplifier to give us a useful output? The answer, as the name implies, is to drive the amplifier differentially.

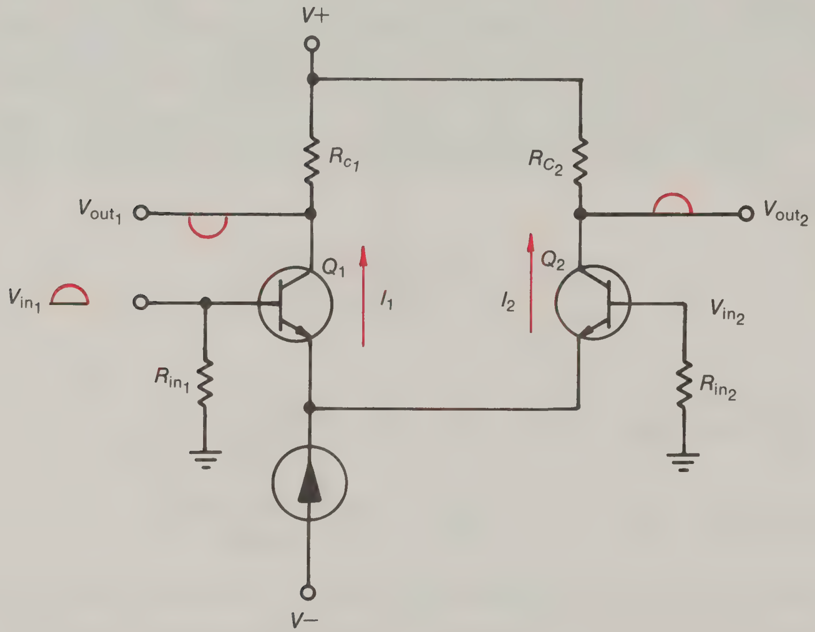


Figure 1-28. A differential amplifier with an input signal applied, producing two separate output signals.

As shown in **Figure 1-28**, with the base of Q_2 grounded and a one volt signal applied to the base of Q_1, Q_1 will conduct harder causing more of the supply current to flow in the Q_1 branch of the differential amp. Therefore, less current flows through the Q_2 branch. With more current flowing through Q_1, R_{C_1} will drop more voltage, causing the voltage level at V_{out_1} to decrease (swing negative). Notice that at the same instance, the current flowing through R_{C2} causes it to drop less voltage, thereby making V_{out_2} more positive.

If the inputs are reversed, the same series of events occur in reverse. Whichever input has a signal applied to it has an output movement in the opposite direction. This is also true with negative values.

With input V_{in_1} grounded, as shown in **Figure 1-29**, a negative voltage is applied to V_{in_1}. Q_1 conducts less, making I_1 less. I_2 has to increase because of the constant current source. R_{C_1} drops less voltage causing the value of V_{out} to increase, while R_{C2} drops more voltage making V_{out_2} swing negative.

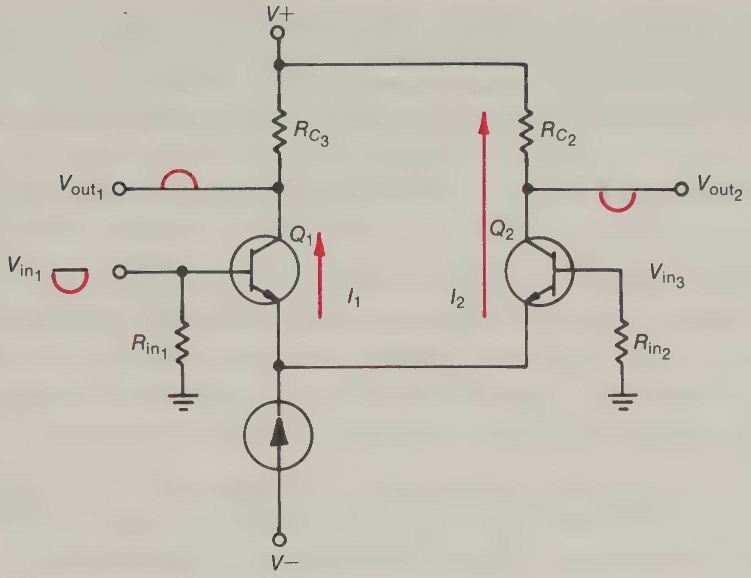

V+
R_{C_3}
R_{C_2}
V_{out_1}
V_{out_2}
Q_1
Q_2
V_{in_1}
V_{in_3}
I_1
I_2
R_{in_1}
R_{in_2}
V−

Figure 1-29. A negative input signal produces opposite output signals.

In many op amps, only one output from the differential amplifier is used. The output from the collector of Q_1 (V_{out_1}) is taken as the output of the differential amplifier stage and fed into the high-gain amplifier/level shifter stages that follow.

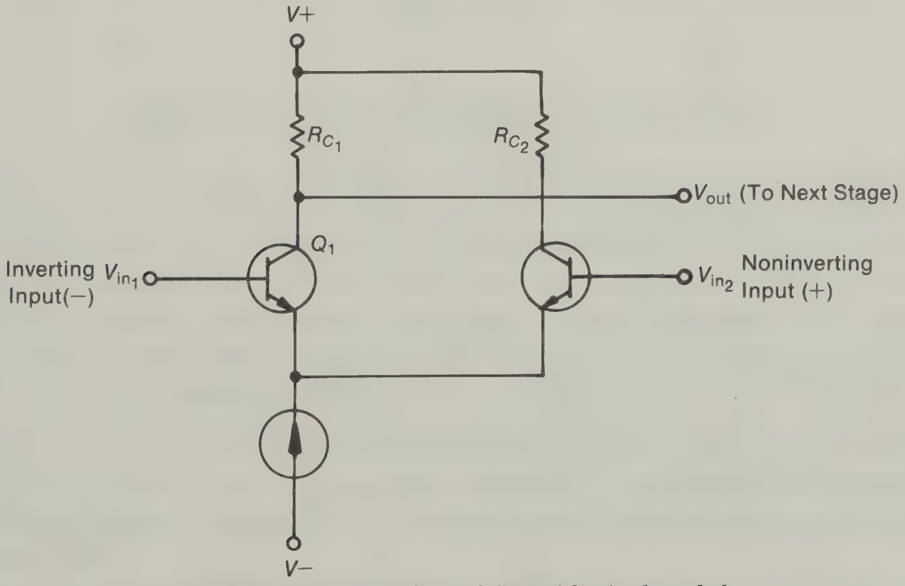

V+
R_{C_1}
R_{C_2}
V_{out} (To Next Stage)
Q_1
Inverting V_{in_1}
Input(−)
V_{in_2} Noninverting
Input (+)
V−

Figure 1-30. A differential amplifier with single-ended outputs which produce inverting and non-invertins inputs.

As we mentioned earlier, there is some value of DC voltage present at the output of the amplifier for a no-input condition. In **Figure 1-30**, any input signal applied to V_{in_2} appears at the output with the same polarity, with respect to the DC level, as it was applied. Therefore, this input is termed the noninverting input and signified by a (+) sign.

Any signal introduced at V_{in_1} appears at the output with an opposite polarity with respect to the DC level. This input is termed the inverting input and is indicated by a (−) sign.

The constant current source and differential amplifier make up the high-impedance input stage of the 741 op amp. The differential amplifier allows the op amp to respond to the difference between two input signals. The common-emitter structure, combined with the high impedence of the constant current source, gives the op amp the extremely high-input impedance which proves so useful in many circuit applications.

There are several operational amplifiers available which use *field effect transistors* (FET's) to provide extremely large input resistances and very low levels of DC bias currents. The operation of these differential amplifiers is nearly identical to the bipolar transistor amplifiers just discussed.

IC manufacturers also cascade (connect the output of one amplifier to the input of a second amplifier) differential amplifier stages to provide increased gain and sensitivity. **Figure 1-31** shows a common method of cascading differential amplifiers.

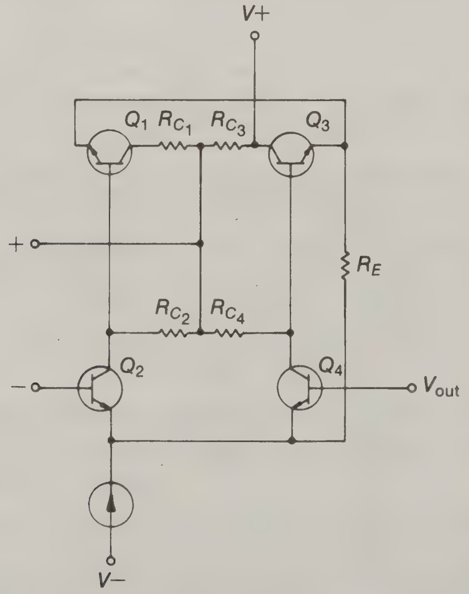


Figure 1-31. Cascaded differential amplifiers.

The double-ended (both collectors) output of the first differential amp stage is applied to the inputs of the second stage, which is used to provide a single-ended output. The two stages are directly coupled and produce a total voltage gain equal to the product of the individual gains. Resistor R_E is necessary to raise the voltage level of emitters Q_3 and Q_4 to nearly the same value as their bases. This prevents the quiescent DC level of the first amplifier from saturating the transistors of the second stage.

The differential voltage level that may be applied to a simple differential amplifier is somewhat limited. **To increase the safe allowable differential potential, the 741 employs a circuit configuration known as a latteral pair, as shown in Figure 1-32.**

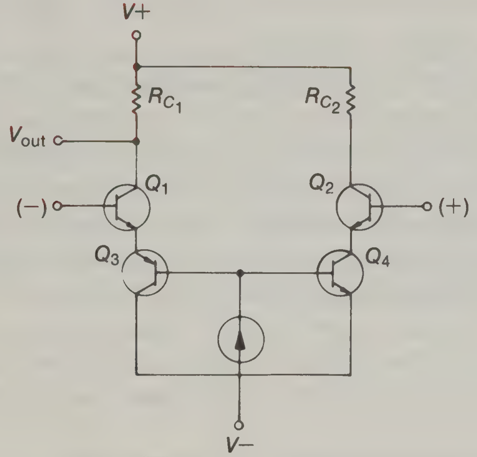


Figure 1-32. A differential amplifier with latteral pairs added.

Transistor Q_3 comprises a lateral pair with Q_1, and Q_4 with Q_2. By placing the PNP transistors in the common emitter leg of the simple differential amplifier, the allowable differential input voltage that may be placed across the two inputs has been greatly increased. The addition of the lateral PNP, which has a large reverse-bias breakdown voltage, means that the input voltage differential would have to break down the reverse-biased, base-emitter junctions in order to damage the amplifier.

Lateral pairs are also used in integrated circuits to increase the current gain of the circuit. This configuration provides no voltage gain. The name "*lateral* pairs" refers to the manner in which these transistors are fabricated. Instead of being constructed vertically on the substrate, these transistor junctions are fabricated side by side on the substrate. Lateral PNP's don't possess the good performance qualities of the vertical NPN.

The open-loop (no feedback) voltage gain of a 741 op amp is approximately 200,000. Most of this gain is developed by a Darlington pair amplifier configuration.

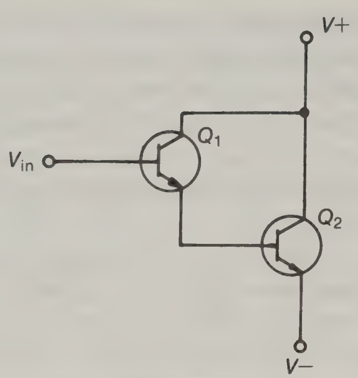


Figure 1-33. A high-gain Darlington Pair configuration.

As shown in **Figure 1-33**, this configuration provides an overall gain (B) for the circuit that is the product of the beta of Q_1 and the beta of Q_2. This is accomplished by injecting the emitter current of transistor Q_1 into the base of transistor Q_2.

It has already been noted that the differential amplifier has some value of DC voltage present at its output, for an input condition of zero volts. DC level shifters are circuits which translate this DC voltage output from the differential amplifier to zero. This is done so the op amp output may swing positive and negative with respect to ground, instead of the differential amplifier's DC level.

The exact type of circuitry used differs from one type of op amp to another, because the exact level shifter design is dependent upon the configuration of the amplifier stages that preceed the level shifter, and the type of output stage it has to drive.

A simplified level shifter is shown in **Figure 1-34.**

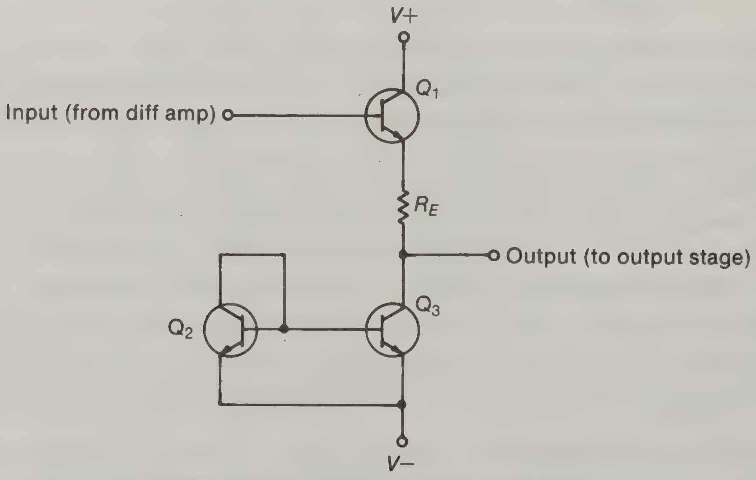


Figure 1-34. A simple DC level shifter.

The DC output, from the collector of the differential amplifier, is applied to the base of Q_1. The base-emitter junction drops approximately 0.6 volts, leaving R_E to drop the remaining value of collector voltage.

$$V_{R_E} = V_{\text{collector}} \text{ (from diff-amp)} - 0.6 \text{ Volts}$$

The value of R_E can easily be calculated since the level shifter is supplied from a constant current source.

$$R_E = \frac{V_{R_E}}{I_{R_E}}$$

With the proper value of R_E, the output level of the op amp will be shifted to zero volts for a no input condition.

As an example, let's say the output of the differential amplifier goes more positive. The base-emitter junction continues to drop 0.6 volts. The constant current source prevents the voltage drop across R_E from changing, so the level shifter output voltage will increase by the same amount as the input signal.

Likewise, if the signal from the differential amplifier swings in a negative direction, the constant current source prevents V_{R_E} from changing, and the level shifter output is forced to swing negative. Notice that the typical level shifter provides no voltage gain but only allows the op amp output to swing positive and negative with respect to ground.

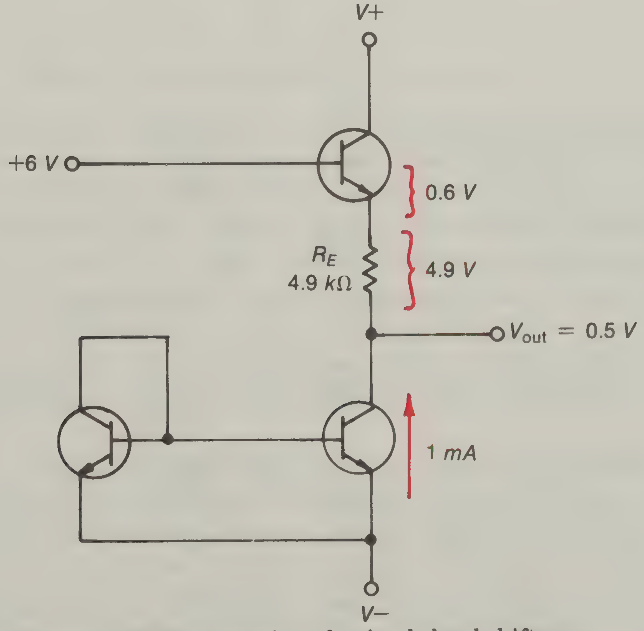


Figure 1-35. The operation of a simple level shifter.

As a practical example, let's say the DC offset voltage from the differential amplifier is +5.5 volts and the level shifter is "anchored" by a 1 mA constant current source. See **Figure 1-35.**

$$V_{R_E} = V_{\text{collector}} - V_{BE}$$

$$V_{R_E} = +5.5 \text{ Volts } -0.6 \text{ Volts}$$

$$V_{R_E} = +4.9 \text{ Volts}$$

$$R_E = \frac{V_{R_E}}{I_{R_E}}$$

$$R_E = \frac{+4.9V}{0.001A} = 4.9\ k\Omega$$

If $V_{\text{collector}}$ increases by +0.5 volts, the output of the level shifter is forced to increase by +0.5 volts.

It is desirable that the output stage of an IC have low-output impedance, and be able to provide high levels of output current, in order to drive large loads. It's also desirable that the output be able to provide voltage swings which can approach the power supply voltages.

A very popular IC output stage configuration is the complementary/symmetry stage, shown in **Figure 1-36.**

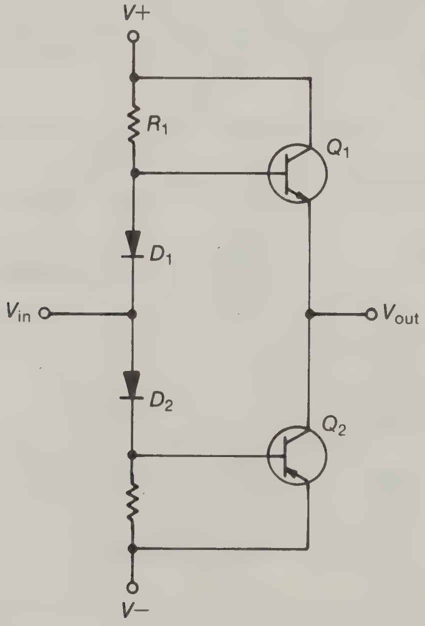


Figure 1-36. A complementary/symmetry output stage

When no load is connected to the output terminal, this configuration draws small quiescent currents from the power supplies. Yet, this circuit is capable of delivering large output currents without significant drops in output voltage. Large output voltage swings are available since the output voltage is prevented from approaching the supply voltages by little more than a forward biased diode drop.

Ideally, equal positive and negative supply voltages produce an output voltage of zero volts when no input signal is applied. When a positive signal is applied to V_{in}, Q_1 will turn on and supply current to the output. Conversely, negative signals will turn on Q_2 and supply output current. This configuration offers no voltage gain but does provide current and power gain.

Another popular output stage used by IC designers is the emitter follower, shown in **Figure 1-37.**

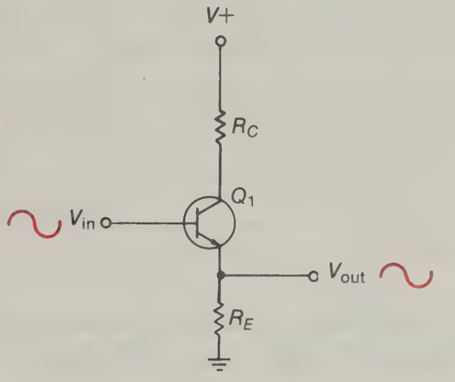


Figure 1-37. An emitter-follower output stage

This type of output stage is used widely in IC's, which operate from single power supply voltages. The physical layout of the circuit resembles the common emitter amplifier, except that the output is taken from the emitter instead of the collector. In operation, this circuit performs quite differently than the common emitter amp.

The emitter follower offers very high levels of input impedance and can be designed to have relatively low levels of output impedance. Due to these qualities, the emitter follower is often referred to as an isolation amplifier. This circuit provides no voltage gain, since the output is always a base-emitter junction voltage drop lower than the input signal voltage. The stage does deliver high levels of current gain and moderate power gain.

In **Figure 1-37**, a positive going input signal increases the forward bias of Q_1, causing the transistor to conduct more current from emitter to collector. As the emitter current increases, emitter resistor R_E drops more voltage which in turn raises the output voltage. Notice that no phase inversion occurs in the emitter follower as it did in the common-emitter amplifier. This configuration is also referred to as a common collector amplifier.

The characteristics of this configuration are: unity voltage gain, high current gain, modest power gain, high input impedance, low output impedance, and no phase inversion.

IC output stages tend to produce heat. For this reason, output stages are commonly placed as far as possible from the input stage on the chip, to reduce the effects of temperature on the circuit.

Topic Review 1-8

1. The ______ ______ was originally developed to respond to the difference between two ______ signals.

2. In **Figure 1-15**, with no signal applied to input V_{in_1} or V_{in_2}, V_{out} will equal ______.

3. In **Figure 1-16**, the ability of the differential pair of transistors, Q_1 and Q_2, to block identical input signals is termed ______ - ______ ______.

4. The ______ ______ ______ and ______ ______ make up the high-impedance input stage of the 741 op amp.

5. ______ ______ ______ are circuits which translate the small value of DC voltage, present at the output of the differential amplifier for zero volts in, to a condition of zero volts out.

Answers:

1. differential amplifier
   input
2. V_{out_2}
3. common-mode rejection
4. constant current source
   differential amplifier
5. DC level shifters

1-9 Summary Points

1. IC's are packaged in plastics, ceramics, or metal canisters. The type of packaging used is usually determined by the environment in which the IC will be used.

2. IC's generally offer much better characteristics and lower cost than similar discrete circuits.

3. Differential amplifiers produce an output voltage which is proportional to the difference of two input voltages.

4. Differential amplifiers can be used with a single-ended input (one input grounded); with a single-ended output (only one output used); with double-ended inputs (using both inputs); with double-ended outputs (using both outputs), or any combination of input/output configurations.

5. Common-emitter amplifiers have a high-input impedance, low-output impedance, high voltage gain, current gain, good power gain, and phase inversion.

6. A Darlington pair configuration provides extremely high current gain and signal sensitivity.

7. Lateral pairs are low performance PNP structures which provide current gain.

8. Differential amplifiers can be cascaded to provide higher gain.

9. It is desirable that output stages have low-output impedance and be capable of large-output voltage swings. They must also be capable of delivering large amounts of output current to drive large loads.

10. Complementary/symmetry output stages have low-quiescent current levels and very large-output voltage swings. They can deliver large amounts of output current.

1-10 Chapter Progress Evaluation

1. What type of transistor is formed in an IC substrate by vertical diffusion, especially where complementary circuits are being fabricated?

2. In the manufacturing of IC's, what process vaporizes aluminum through a mask to create wiring interconnections and crossovers?

3. An N-channel depletion MOSFET consists of a ________ substrate into which two $N+$ buttons and a lightly doped ________ channel have been diffused.

4. In the IC identification number, 3N 74 ALS 00J, the ALS stands for

5. ______ packaged IC's are noted for their ability to operate at high temperatures.

6. Two characteristics of the common-emitter amplifier are:

7. Current gain of a common-emitter amplifier is a measure of a change in ______ current to a change in ______ current, with V_{CE} held constant.

8. This current gain is also referred to as:

9. If the amplifier in **Figure 1-14** has a change in I_C of 1.5 mA when I_B changes by 20 μA, what is the Beta?

10. The use of a constant-voltage reference in IC's is to provide a constant level of voltage, despite the variations in:

11. Figure the common mode rejection ratio for an op amp if you're applying a 100 microvolt input signal, which results in a differential mode output of 10 volts and

12. ______ are circuits which translate the DC output from the differential amplifier stage of the standard op amp to zero volts.

Chapter 2

IC Operational Amplifier

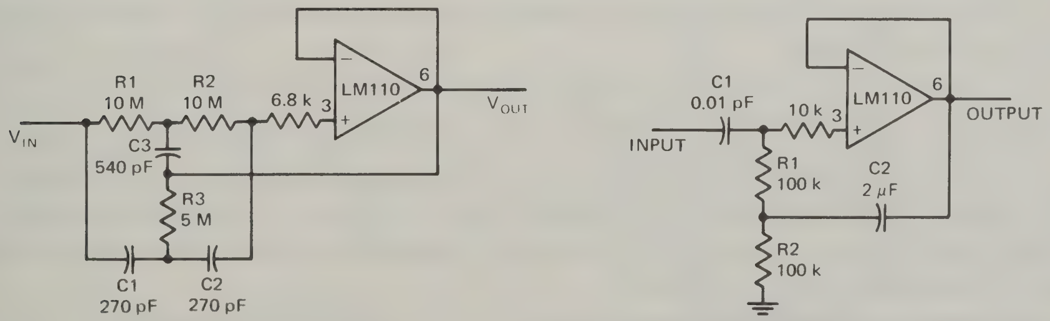
Objectives

Upon completion of this chapter, you should be able to do the following:

- List and define the electrical characteristics and parameters of IC operational amplifiers.
- Describe the operation and construction of inverting and noninverting IC operational amplifiers.
- List several power supply considerations in conjunction with IC op amps.

2-1 Introduction

The most popular IC device is the *operational amplifier* (known to the trade as an *op amp*), because of its low cost, small size, and versatility. A typical op amp has some noteworthy characteristics, such as high input impedance, low output impedance, infinite voltage gain, flat frequency response within frequency range, zero input signal, and zero output level. Op amps are operated from either single or split power supply voltages and can be found in communications, computers, measuring instruments and electronic displays. There are literally hundreds of applications for op amps, and numerous types of op amp IC's. Some typical examples are shown in **Figure 2-1.**



HIGH-Q NOTCH FILTER *HIGH-INPUT-IMPEDANCE A-C AMPLIFIER*

Figure 2-1. IC op amp applications

The most important points to remember about an op amp are its high input impedance, its extremely low output impedance, and the fact that gain can be varied by using resistors of different value in an output-to-input feedback loop. A closed loop or *feedback* as it's called will be discussed later in this chapter.

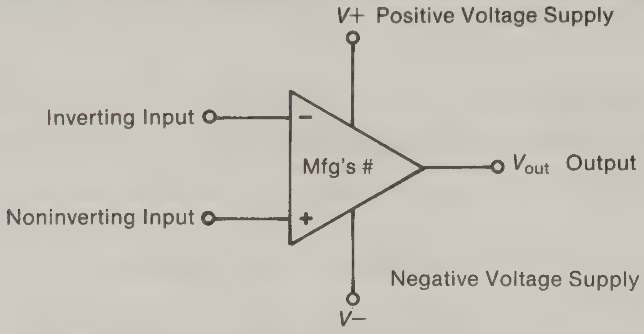


Figure 2-2. Operational amplifier schematic symbol.

The schematic symbol depicted in **Figure 2-2** is that of a typical operational amplifier, showing its major terminals. The op amp has two input terminals: the inverting input, indicated by a minus (−) sign, and the noninverting input, indicated by a plus (+) sign. The output terminal is shown extending from the point of the triangle; opposite the input terminals. Other package leads are not always shown on the schematic symbol. When power supply, frequency compensation, or nulling leads are included, they are shown extending above and below the symbol. Whether the power supply connections are shown or not, it should be understood that they are always physically made so the chip can operate. On the other hand, the minor terminals may not be used at all.

Op Amps and other integrated circuits are manufactured by the monolithic fabrication process. With this process, anywhere from ten to tens of thousands of transistor and diode (active) elements are formed on or within a single piece of substrate (i.e., silicon). Resistive and capacitive (passive) elements are usually formed along with the active elements.

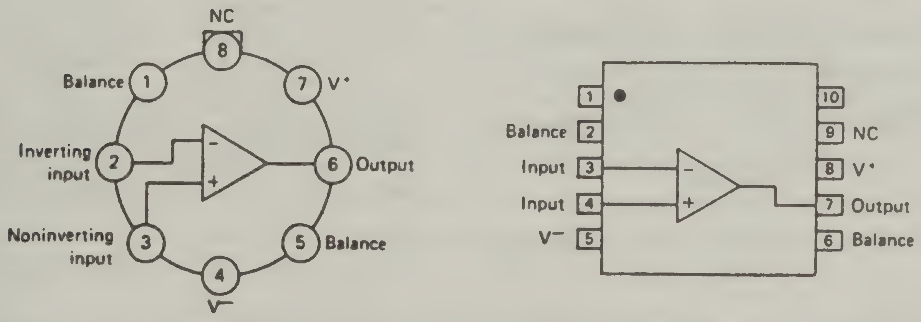
IC resistors are formed in the same manner as the base diffusion in an NPN transistor. The resistance element is a piece of *P*-type material, wound back and forth to take up as little space as possible on the silicon wafer. Resistive elements in integrated circuits are kept to a minimum, both in number and in total resistance value, because resistance takes up valuable space on the chip and creates heat. So, the less total resistance needed for the circuit to operate properly, the smaller the total surface area of the silicon wafer.

Integrated circuit capacitors are formed in a variety of ways. The most common technique is to simply utilize the capacitance of a reverse-biased diode junction. Total capacitance in integrated circuit design is also kept to a minimum.

There are no inductors in integrated circuits. In circuits where inductance is necessary, it must be simulated. External inductors may be used if absolutely necessary.

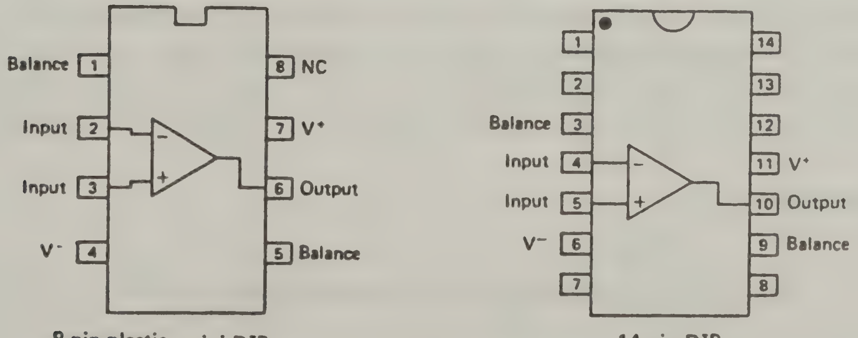
To offset these limitations, IC designers use many of the inherent qualities of the monolithic fabrication process. For example, since the entire chip is formed at one time, and from the same material, the designer can maximize the use of identical components. Also, whenever possible, the designer substitutes transistor and diode configurations for larger area components, such as resistors and capacitors. And, while absolute values are hard to predict, relative values of resistance, capacitance, voltage, and current gain can be established in an IC; with an extremely high degree of accuracy.

IC op amps are manufactured in a wide variety of package configurations. **Figure 2-3** shows a collection of single (1), dual (2), and quad (4) op amp packages and pin configurations. Single op amps may come in 8-pin metal cannister, 10-lead low-profile plastic, ceramic or glass/metal flat-pack, and 8 or 14-pin dual-in-line package (DIP) configurations. Dual op amps can come in 10-lead metal cannister, 14-lead flat-pack, and 14-pin DIP arrangements. Quad op amps come in 14-pin dual-in-line packages.


NC
8
Balance
1
7
V⁺
Inverting input
2
−
+
6
Output
Noninverting input
3
5
Balance
4
V⁻
1
10
Balance
2
9
NC
Input
3
8
V⁺
Input
4
7
Output
V⁻
5
6
Balance

TO-5

Flat package


Balance
1
8
NC
Input
2
7
V⁺
Input
3
6
Output
V⁻
4
5
Balance
1
14
2
13
Balance
3
12
Input
4
11
V⁺
Input
5
10
Output
V⁻
6
9
Balance
7
8

8-pin plastic mini-DIP

14-pin DIP

Figure 2-3. Op amp package configurations
Courtesy of National Semiconductor Corp.

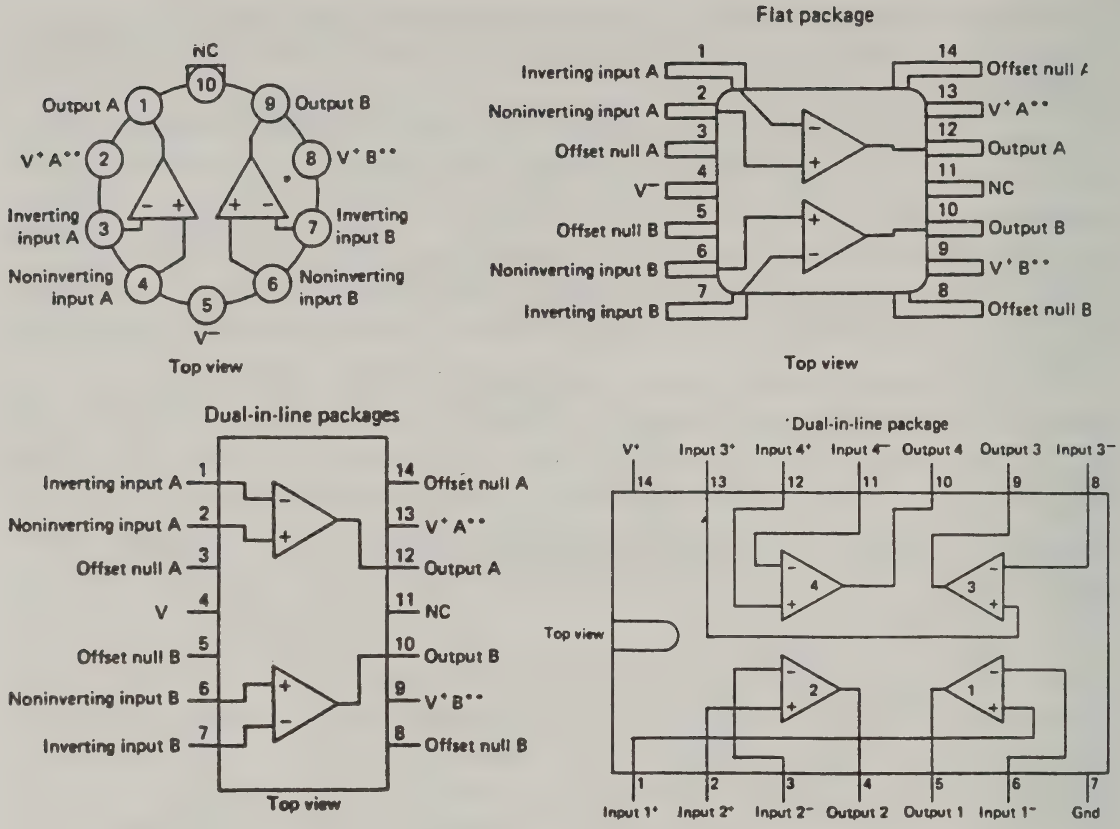

Flat package
NC
Output A
Output B
V⁺A**
V⁺B**
Inverting input A
Inverting input B
Noninverting input A
Noninverting input B
V⁻
Top view
Inverting input A
Noninverting input A
Offset null A
V⁻
Offset null B
Noninverting input B
Inverting input B
Offset null A
V⁺A**
Output A
NC
Output B
V⁺B**
Offset null B
Top view
Dual-in-line packages
Inverting input A
Noninverting input A
Offset null A
V
Offset null B
Noninverting input B
Inverting input B
Offset null A
V⁺A**
Output A
NC
Output B
V⁺B**
Offset null B
Top view
Dual-in-line package
V⁺
Input 3⁺
Input 4⁺
Input 4⁻
Output 4
Output 3
Input 3⁻
Top view
Input 1⁺
Input 2⁺
Input 2⁻
Output 2
Output 1
Input 1⁻
Gnd

Figure 2-3. (Continued)

The terminal connections previously discussed should be easily recognized in the pin-out figures. Positive and negative supply voltages are indicated by *V*+ and *V*− respectively. The inverting, noninverting, and output terminals are clearly marked. The pins marked *offset null* are covered later in the chapter. The pins marked “NC” are not connected to the chip, but are included to give support to the package.

Topic Review 2-1

1. IC ______ ______ are inexpensive, reliable, easy to use circuits.

2. Applications of op amps include: communications, ______, ______ ______, and electronic displays.

3. The op amp has two input terminals: the ______ input, indicated by a (–) sign, and the ______ input, indicated by a (+) sign.

4. Some op amps operate from a single power supply voltage, while others operate from a ______ supply.

5. IC op amps come in ______, ______, and ______ packages and pin configurations.

Answers:

1. op amps
2. computers, measuring instruments
3. inverting, noninverting
4. split
5. single, dual, quad

2-2 The Basic Op Amp

It is not necessary to know what all of the internal components of an integrated circuit do in order to use it. Frankly, if a chip goes bad, there is no way to repair it. So, the only information really needed to use any integrated circuit is an understanding of how the chip functions as a whole, its working limitations, and how to wire the external components around the IC to achieve the desired results. In this topic, we will concentrate on the first point and begin with a general circuit explanation.

Figure 2-4 is a schematic diagram of a simplified operational amplifier, with a complementary-symmetry output stage.

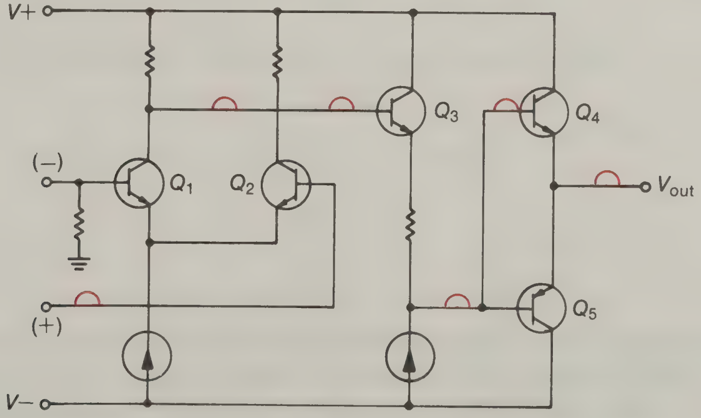


Figure 2-4. A simplified operational amplifier.

When the input signal is positive on the noninverting (+) input, the emitter of Q_2 swings positive by the same amount, because Q_2 is an emitter follower. Notice the emitter of Q_2 is directly coupled to the emitter of Q_1. As the emitter of Q_1 swings positive, the collector of Q_1 swings positive, since Q_1 is configured as a common-base amplifier.

This output signal is then fed to the base of Q_3, the DC level shifter (emitter follower). The positive output from its emitter, is fed to the bases of Q_4 and Q_5. This positive signal on the base of Q_4, an NPN transistor, causes it to turn on, driving it into saturation. Q_5, a PNP transistor, is driven into cut-off. This action places V_{out} at positive saturation or $V+$, minus the small internal voltage drop of the output stage.

Likewise, if a positive signal were applied to the inverting (−) input, the differential amplifier would invert the signal. The inverted signal would cut off the NPN transistor and cause the PNP transistor to saturate, driving the op amp output to its negative saturation level.

It should be evident that if negative voltage signals had been applied, the outputs would have been driven in the opposite direction.

The stages within the IC op amp fall into four general categories: constant current and voltage sources, amplifiers, level shifters, and output stages. To better understand how op amps accomplish their design intentions, let's look at the National Semiconductor LM741 operational amplifier.

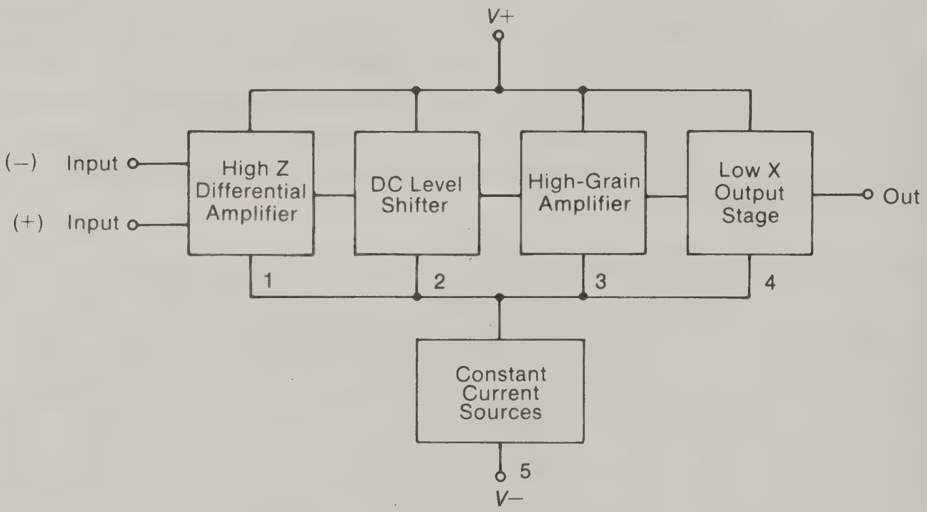


Figure 2-5. A block diagram of the 741 op amp.

The block diagram in **Figure 2-5** shows the arrangement of the LM741 op amp's basic stages. These stages were covered in detail in Chapter 1. A point of interest in **Figure 2-5** is that the LM741 operates with a *split* power supply (*V*+ and *V*−), allowing the op amp's output to swing positive and negative with respect to ground.

A full schematic diagram of the 741 operational amplifier is shown in **Figure 2-6.**

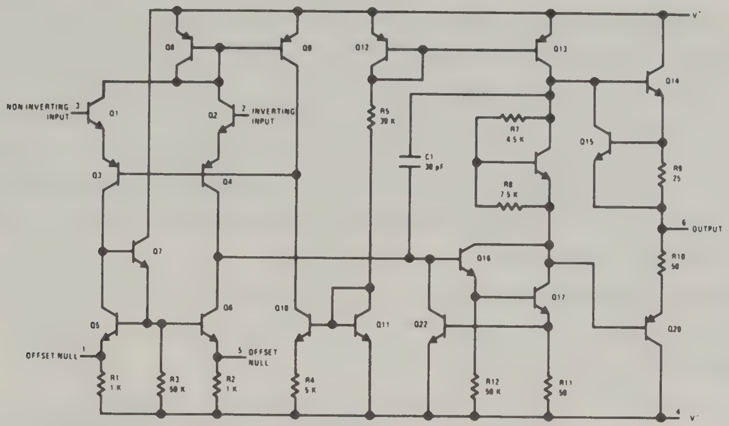

Q8
Q9
Q12
Q13
V+
Q14
NON INVERTING INPUT 3
Q1
Q2
2 INVERTING INPUT
R5 39 K
R7 4.5 K
Q15
C1 30 pF
R9 25
R8 7.5 K
Q3
Q4
6 OUTPUT
Q7
Q16
R10 50
Q17
Q5
Q6
Q10
Q11
Q22
Q20
OFFSET NULL 1
5 OFFSET NULL
R1 1 K
R3 50 K
R2 1 K
R4 5 K
R12 50 K
R11 50
4 V-

Figure 2-6. The 741 op amp.
Courtesy of National Semiconductor Corporation

You may notice that the 741 utilizes a complementary-symmetry output stage. This is because of its low output impedance and ability to drive large loads without significant change in output voltage.

Topic Review 2-2

1. Placing a positive signal on the noninverting input of an IC op amp causes its output voltage to go to its ______ saturation point.

2. A negative voltage signal on the inverting input of an IC op amp causes its output voltage to go to its ______ saturation point.

3. IC op amp stages fall into four general categories: constant ______ and ______ sources, ______, ______ ______, and output stages.

4. The 741 op amp operates from a ______ power supply.

Answers:

1. positive
2. positive
3. current, voltage,
   amplifiers, level shifters
4. split

2-3 The Ideal Op Amp

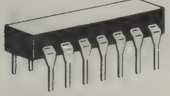
Ideally, op amps should posses the following characteristics: infinite input impedance, maximum gain and bandwidth, zero output impedance, zero output for zero input (or no offset), and no change of performance with temperature change.

However, there are no *ideal* op amps, and each type has its own individual set of operating characteristics. As stated in the previous topic, it is important to know the working limitations of the chip. To assist in the selection of the op amp best suited for a specific application, IC manufacturers provide date sheets listing typical operating characteristics and limitations.

The electrical characteristics from the data sheet for the 741 is shown in **Figure 2-7.** It is a very valuable tool when working with integrated circuits, and it is important to understand the information presented.

PARAMETER	CONDITIONS	LM741A/LM741E			LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ C$										
	$R_S \leq 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \leq 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 50\Omega$			4.0							mV
	$R_S \leq 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25^\circ C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25^\circ C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25^\circ C$		30	80		80	500		80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25^\circ C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25^\circ C$							±12	±13		V
	$T_{AMIN} \leq T_A \leq T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25^\circ C$, $R_L \geq 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V

Figure 2-7. The manufacturer's data sheet for the 741 op amp
Courtesy of National Semiconductor Corp.



Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} < T_A \le T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \le 50\ k\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \le 50\Omega$	86	96								dB
	$R_S \le 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$			150							mW
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Figure 2-7. (Continued)

The 741 data sheet also contains information such as a description of the device, a list of outstanding features and typical applications, package types, pin configurations and a schematic of the chip. Perhaps two of the most valuable pieces of information the data sheet offers the designer, engineer or technician is the absolute maximum ratings, and electrical characteristics (parameters) of the device. Let's examine some of the more important parameters of a real world op amp, while keeping in mind the *ideal* version.

Input impedance: This is the value of measured resistance between the two input terminals of the op amp. Usually, the higher the input impedance, the better the overall performance of the op amp. Op amps with FET inputs have input impedances of 1 megohm or better.

Output Impedance: *Output impedance* is the resistance that can be measured from the op amp output to ground. Typical output impedance for the 741 is 75Ω. When the op amp is used with feed-back, the effective output impedance is reduced to very nearly zero ohms. Output impedances range from 25 ohms to a few thousand ohms, depending on the type of op amp.

Input Capacitance: *Input capacitance* becomes important at higher frequencies. This is a measure of capacitance at one input terminal when the other is grounded.

Input capacitance for the 741 op amp is typically less than 2 picofarads.

Input Offset Voltage: The output of the *ideal* op amp would be zero when no input signal is applied to the input terminals. However, due to the extremely high gain of the op amp, even a slight circuit imbalance can cause an output voltage. Even though the chip's components are extremely well matched, they're not perfect, so the output will not be zero when there is no input signal, unless there is some offset compensation. The amount of voltage that must be applied to offset one of the inputs, to bring the output to zero, is the *input offset voltage.* Environmental conditions can also be responsible for input offsets. Induced noise voltage, in the micro-volt range, from sources such as flourescent lighting, external circuitry, etc., are sufficient to drive the op amp output to saturation.

To allow the user to compensate for the effects of offset, manufacturers include external offset null pins in some op amp packages. Not all op amps are equipped with nulling capabilities, and in these cases offset compensating networks must be constructed in the input circuit. This topic will be covered in more detail, later in this chapter.

Input Offset Current: Ideally, both input currents should be equal to obtain a zero volt output. However, due to circuit imbalances, a small offset current is usually required. *Input offset current* is the difference between the currents, into or out of the input terminals, when the output voltage is zero. Input offset current may range up to 20 mA in some op amps while the 741 has a typical input offset current of around 20 nA.

Input Bias Current: In the *ideal* op amp, with infinite input impedance, no current flows into or out of its inputs. Real op amps require some input current to operate. Due to the very high input impedance of the op amp, input bias current is limited to the micro/pico amp range. *Input bias current* is expressed as the average of the two input currents, with no input signal applied.

$$I_B = \frac{I_{B_1} + I_{B_2}}{2} \tag{2-1}$$

Changes in temperature tend to affect this current. Temperature changes will affect offset currents and voltages, and will upset any "adjusted" op amp, producing output voltage errors. These errors, due to temperature changes, are termed *drift.* Generally, the lower the input bias current, the smaller the output voltage error.

Power Dissipation: *Power dissipation* is the amount of power the op amp consumes at quiescence (no input signal applied). Typically the 741 consumes 85 mW with a ±20 volt power supply.

Large Signal Voltage Gain: Operational amplifiers amplify the voltage difference between the two input terminals. Therefore, the voltage gain of an operational amplifier is:

$$A_v = \frac{V_{out}}{V_1 - V_2} \tag{2-2}$$

This is the open-loop (no feedback) gain of the amplifier at zero hertz or DC. The output voltage is much larger than the input voltage. For the 741, the output voltage will typically be 200,000 times larger than the differential input voltage. The maximum output voltage swing of the op amp is limited to approximately 90 percent of the voltage supply, due to the internal voltage drops of the amp. At this point, the output is said to be in plus or minus saturation ($\pm V_{sat}$). The consequence of all this is that for a typical 741 operating with a ±12 volt supply, the output will be driven to saturation when the differential input voltage is about 55 microvolts.

$$A_v = \frac{V_{out\,(max)}}{V_1 - V_2}$$

$$\text{or: } V_1 - V_2 = \frac{V_{out\,(max)}}{A_v}$$

$$\text{so: } V_1 - V_2 = \frac{10.8\,V}{200{,}000} = 54\,\mu V \tag{2-3}$$

Again, this is the open-loop gain of the op-amp. In most cases, feedback or a closed-loop is used, as will be seen later in this and the following chapters.

Slew Rate: *Slew rate* is defined as the maximum rate of change in output voltage for a change in input voltage. It is stated in volts per microsecond. This can be expressed as:

$$\text{SR} = \frac{\Delta V_{out}}{\Delta t} \tag{2-4}$$

Slew rate (SR) is an indication of how rapidly the op amp's output can change in response to a change in input. The effects of slew rate become evident in high frequency or high rates of signal change applications, such as filters, oscillators, and computer related operations, where rapidly changing signals tend to be distorted (see figure 2-8).

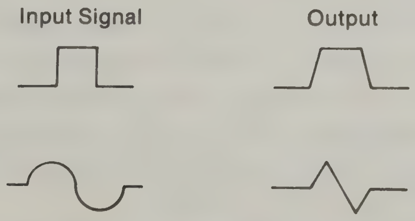


Figure 2-8 The effects of slewing.

The 741 has a relatively low slew rate ($0.5 V/\mu sec$), which tends to limit its use in higher frequency applications. For these applications, there are several op amps with significantly better slew rates. Slew rate is usually specified at unity gain (or a gain of +1), because the slew rate will change with a change in voltage gain.

Frequency Compensation: The internal stages of the op amp are direct coupled. Due to the high gain and phase shifting between the internal stages, some form of *frequency compensation* may be necessary to prevent the op amp from becoming an oscillator. The 741 comes with an internal frequency compensating capacitor. Other op amps may require external compensation capacitors. These capacitors decrease the gain of the op amp as the signal frequency increases.

Frequency Response: Manufacturers specify the large signal voltage gain of the op amp at DC, with no feedback applied. The gain of the op amp decreases as frequency increases. **Figure 2-9** shows a typical performance curve of voltage gain, as a function of frequency for the 741.

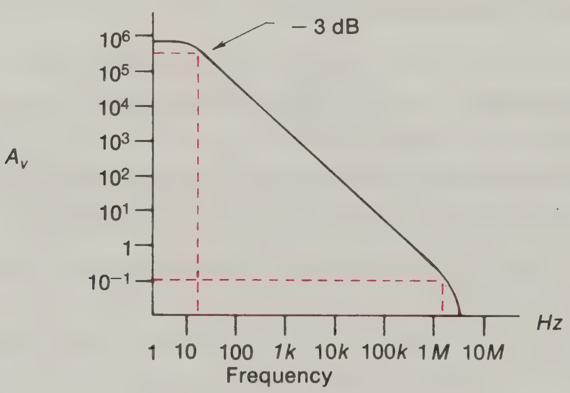


Figure 2-9. A bode graph.

It may be seen from **Figure 2-9**, that as frequency increases by a factor of ten (a decade), the gain of the circuit decreases by a factor of ten. The bandwidth of a circuit is the range of frequencies which generate an output greater than 70.7 percent (3 dB) of the maximum output. The bandwidth of the 741 op amp is only about 10 *Hz* in the open-loop mode. Fortunately, linear applications of the op amp use degenerative feedback to reduce the high gain of the op amp. In these applications, the bandwidth of the op amp is increased. When feedback is used to control gain, the bandwidth can be calculated by the gain-bandwidth product from the graph. The gain-bandwidth product is always equal to the unity-gain frequency of the op amp. The op amp's unity-gain frequency is the frequency at which the gain drops off to a factor of 1. The unity-gain frequency is specified in the data sheet and is approximately 1 *MHz* for the 741. Gain-bandwidth product may be stated:

$$\text{GBP} = \text{Gain} \times \text{Bandwidth} = \text{Unity Gain Frequency} \tag{2-5}$$

As an example; a 741 operating with a gain factor of 10, has a bandwidth of 100 kHz. This is shown in the following calculation:

$$\text{first, GBP} = 1\ MHz = \text{Unity Gain Frequency}$$

$$\text{then, } 1\ MHz = 10 \times \text{Bandwidth (BW)} \tag{2-6}$$

$$\frac{1\ MHz}{10} = \text{BW} \tag{2-7}$$

$$\text{therefore, } 100\ kHz = \text{BW}$$

Common Mode Rejection Ratio: CMRR is a ratio of the differential voltage gain to the common-mode voltage gain.

$$\text{CMRR} = \frac{A_{v\,(\text{diff})}}{A_{v\,(\text{cm})}} \tag{2-8}$$

Power Supply Rejection Ratio: PSRR is the change in the op amp's input offset voltage, due to variations in supply voltages. **PSRR** is expressed in microvolts per volt:

$$\text{PSRR} = \frac{\Delta V_{\text{in(offset)}}}{\Delta V} = \mu\text{Volt/Volt} \tag{2-9}$$

Typically the 741 has a PSRR of $30\mu V/V$. This indicates that the input offset voltage will change $30\mu V$ for each volt of change in the power supply voltage. Another term for PSRR is *supply voltage rejection ratio* (SVRR). Obviously, the lower the PSRR, the better the performance of the op amp.

Supply Current: *Supply current* is the current drawn from the power supply by the op amp. For the 741, supply current is typically 1.7 mA.

Output Short Circuit Current: The 741 series op amps come with built-in short circuit protection. The 741 is guaranteed to withstand 25 mA of current. The output short circuit duration is specified as indefinite, but the op amp's output should not be allowed to remain in this condition for extended periods.

Transient Response: *Transient response* or *response time* is the time required for the op amp's output to change after an input voltage change. Ideally, the op amp would respond instantly to changes of input. Transient response is divided into two sub-sections: *rise time* and *overshoot.*

Rise Time is the time required for the op amp's output to change from an existing value to 90% of a new value, after an input change. As the output approaches the new value, it overshoots this new level before eventually settling down to a steady state.

Overshoot is expressed as "the ratio of the amount of overshoot to the steady state deviation (amount of output change) as a percentage." See **Figure 2-10.**

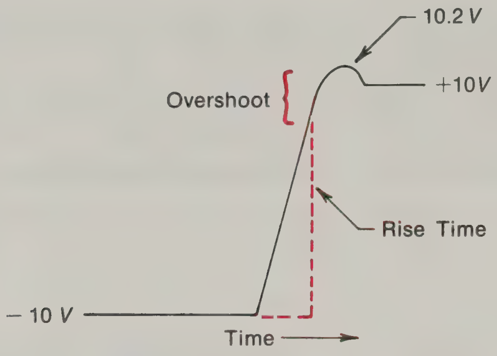


Figure 2-10. Output response characteristics.

$$\text{Overshoot} = \frac{\text{Amount of Overshoot}}{\text{Steady State Deviation}} \tag{2-10}$$

$$= \frac{.2V}{20V} \times 100$$

$$= 1\%$$

Latch-Up: *Latch-up* is a problem which occurs in older op amps when they are driven to saturation. These op amps produce positive feedback, which keeps the op amp in saturation. The output is said to be *latched-up* in this condition. Special precautions must be taken with these op amps to prevent latch-up. The 741 has internal latch-up prevention.

The **absolute maximum ratings** are the outermost limits a particular device can be safely subjected to. The absolute maximum ratings of the op amp are interpreted as follows:

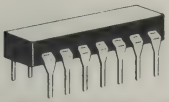
Supply Voltage: The maximum allowable positive and negative supply voltages that may be applied to the op amp. For the 741, the maximum supply voltages are plus and minus 22 volts.

Power Dissipation: The amount of power the op amp can continuously dissipate without damaging the IC. The 741, 8-pin mini-DIP can safely dissipate 310 mW at an ambient temperature of 70° C.

Differential Input Voltage: The maximum voltage that can be placed across the input terminals.

Input Voltage: The maximum voltage, referenced from ground, which can be applied to either input.

Storage Temperature Range: The range of temperatures over which the device may safely be stored.



Operating Temperature Range: The temperature range over which the manufacturer guarantees the op amp's performance specifications.
Pin Temperature (Soldering): The temperature and time period the op amp will withstand when soldering.
Output Short Circuit Duration: The amount of time the op amp can withstand a direct short from the output to ground, or output to either supply.

As evidenced from the aforementioned specifications, the real world op amp and the *ideal* concept are not the same.

Topic Review 2-3

1. All ideal op amps would have infinite ______ ______, ______ and bandwidth, zero ______ impedance, zero output for zero input, and no performance change with a change in temperature.
2. Some of the most important pieces of information on an IC data sheet are the ______ ______ ratings, and electrical characteristics (parameters) of the device.
3. The amount of voltage that must be applied to offset one of the inputs, to bring the output to zero, is the ______ ______ voltage.
4. ______ ______ current is expressed as the average of the two input currents, with no input signal applied.
5. Slew rate is defined as the maximum rate of change in output ______, for a change in input voltage.
6. ______ ______ or response time is the time required for the op amp's output to change after an input change.
7. The maximum voltage that can be placed across the input terminals of the op amp is termed ______ ______ ______, and must never exceed the magnitude of the supply voltages.

Answers:

1. input impedance,
   gain, output
2. absolute maximum

3. input offset
4. Input bias
5. voltage
6. Transient response
7. differential input voltage

2-4 The Inverting Amplifier

As stated earlier, it is important to know how discrete components are used in conjunction with IC op amps, to achieve a desired result. The two most basic circuits are the inverting and noninverting amplifiers. We will cover the noninverting amplifier configuration in **Topic 2-5**.

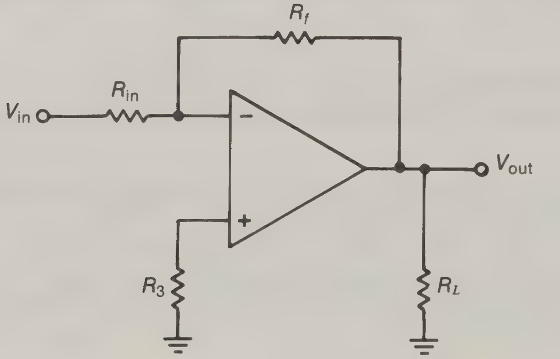


Figure 2-11. An inverting amplifier

With an inverting amplifier, the input signal is fed to the inverting pin (−) of the IC, as shown in **Figure 2-11**. The noninverting pin (+) is tied to ground through R_3, while feedback or the closed loop occurs through R_f. With the inverting amplifier, feedback (V_{out}) is 180° out of phase with V_{in}.

The degenerative feedback holds the voltage level at the inverting input to nearly 0 volts or *virtual ground*. Virtual ground is defined as: "a point that is at 0 volts with respect to ground, but is physically isolated from ground" Actually, the inverting input is at a potential of a few microvolts. This is amplified by the high gain of the op amp to produce an inverted output signal and keep the circuit functioning. If the inverting input was actually at ground, the amplifier wouldn't work at all. How does the op amp maintain the virtual ground condition? Let's increase the input voltage to the inverting amplifier. This positive going input will drive the output signal further negative. The increased negative feedback through R_f will counter the input signal and maintain the virtual ground condition.

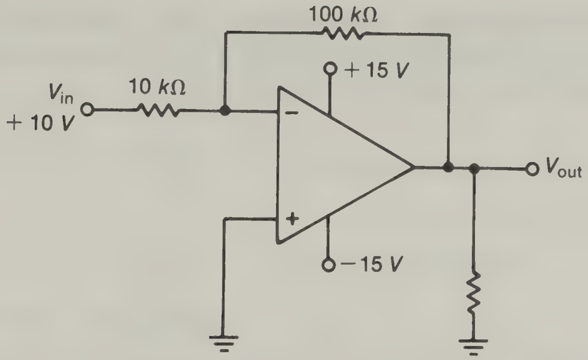


Figure 2-12. A functional model

Theoretically, since the input impedance of the op amp is infinite, no current enters or leaves the inverting input. A +1 volt signal applied to the the input (V_{in}) of **Figure 2-12** would be dropped across R_{in}, causing $1mA$ of current to flow. Because current doesn't flow in or out of the inverting input, the current flows through R_f. The voltage across R_f would then equal:

$$V_{R_f} = I_{R_f} \times R_f \qquad (2\text{-}11)$$

$$V_{R_f} = 1mA \times 10k\Omega$$

$$V_{R_f} = 10 \text{ volts}$$

The gain of the amplifier is determined by the ratio of R_f to R_{in} (inverted), because the same current flows through both resistors. Therefore, the gain of the op amp, or A_v, can be found from:

$$\text{since: } V_{in} = I_{in}\,(R_{in}) \qquad (2\text{-}12)$$

$$\text{and: } V_{out} = I_{in}\,(R_f) \qquad (2\text{-}13)$$

$$\text{and: } A_v = \frac{V_{out}}{V_{in}} \qquad (2\text{-}14)$$

$$\text{by substituting: } A_v = \frac{I_{in}\,(R_f)}{I_{in}\,(R_{in})} \qquad (2\text{-}15)$$

$$\text{therefore: } A_v = \frac{R_f}{R_{in}} \qquad (2\text{-}16)$$

However, there are some loads whose operation is not voltage dependent, but instead must have their current requirements met to operate properly. Every op amp has a maximum current rating that must be observed, and there are two current requirements placed on the op amp. There is the current required by the load, and the feedback current required by the op amp itself. The two currents can be calculated independently by Ohm's Law and simply added together.

$$\text{Load Current } I_L = \frac{V_{\text{out}}}{R_L} \tag{2-17}$$

$$\text{Feedback Current } I_f = \frac{V_{\text{out}}}{R_f} \tag{2-18}$$

$$\text{Output Current } I_{\text{out}} = I_f + I_L \tag{2-19}$$

Since the input signal "sees" ground potential (virtual ground) at the inverting input, the input impedance of the circuit is equal to the value of R_{in}.

As an example:

Design an inverting amplifier with a gain of 15 and an input impedance of 10 $k\Omega$.

$$\text{because: } A_v = -\frac{R_f}{R_{\text{in}}}$$

$$15 = -\frac{R_f}{10\ k\Omega}$$

$$\text{then: } 15\,(10\ k\Omega) = R_f$$

$$\text{finally: } R_f = 150\ k\Omega$$

Topic Review 2-4

1. With an inverting amplifier, the input signal is fed to the ______ pin of the IC.

2. ______ feedback is used to hold the voltage level at the inverting input to nearly 0 volts

3. ______ ______ is defined as: "a point that is at 0 volts with respect to ground, but is physically isolated from ground."

4. The ______ of the amplifier is determined by the ratio of R_f to ______.

5. Two current requirements that an op amp must meet are those required by the ______ and the ______ ______ itself.

Answers:

1. inverting
2. Degenerative
3. Virtual ground
4. gain, R_{in}
5. load, op amp

2-5 The Noninverting Amplifier

There are applications where signal inversion is undesirable. There are also several applications that require a high input impedance. Recall that with the inverting amplifier, all of the input voltage was dropped across R_{in}. As far as the circuit was concerned, R_{in} was the input impedance of the inverting amplifier.

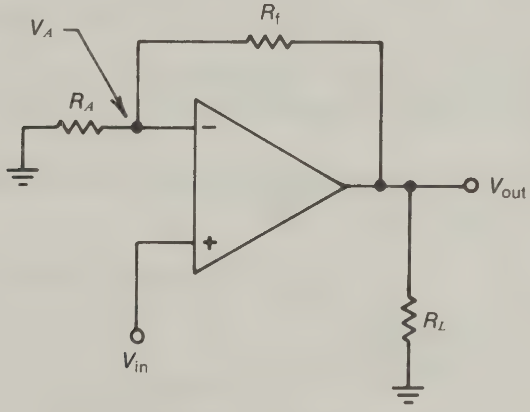


Figure 2-13. A noninverting amplifier.

In the noninverting amplifier configuration of **Figure 2-13**, the input impedance of the circuit is the input impedance of the op amp. Degenerative feedback is still applied to the inverting input to control gain, but V_{in} is applied to the noninverting input; so no phase inversion occurs.

Resistors R_A and R_f provide the feedback current path. The op amp will hold voltage V_A at nearly the same potential as V_{in}, due to the op amp's tendency to maintain zero volts differential, in the closed-loop mode. This allows us to state that V_A (which is dropped across R_A to ground) is approximately equal to V_{in}.

$$V_A \cong V_{in} \tag{2-20}$$

Since R_f and R_A form a resistive voltage divider with V_A held equal to V_{in}, the circuit may be analyzed in terms of the general voltage divider formula.

$$V_{in} = V_A = \frac{R_A}{R_A + R_f(V_{out})} \tag{2-21}$$

$$\frac{V_{in}}{V_{out}} = \frac{R_A}{R_A + R_f} \tag{2-22}$$

The gain of a circuit is determined by $\frac{V_{out}}{V_{in}}$, so by inverting both sides of the equation:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{R_A + R_f}{R_A} \tag{2-23}$$

$$A_v = \frac{R_A}{R_A} + \frac{R_f}{R_A}$$

$$A_v = \frac{R_f}{R_A} + 1$$

therefore: $$V_{out} = \left(\frac{R_f}{R_A} + 1\right) V_{in} \tag{2-24}$$

Remembering a few of the unwanted inherent characteristics of IC op amps; we will look at their compensation networks.

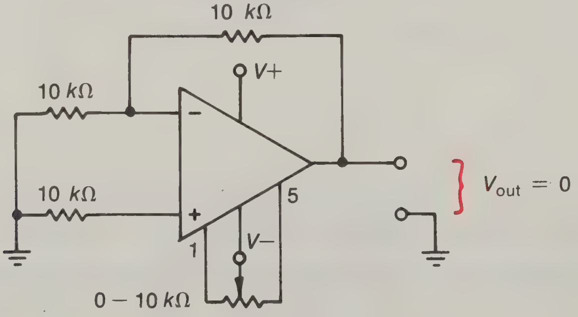


Figure 2-14. Op amp nulling configuration.

The null adjusting arrangement shown in **Figure 2-14** is for op amps equipped with external null pins. This circuit will handle the input offset voltage condition explained in **Topic 2-3**.

To null the op amp, all input signals are removed and a potentiometer is placed between the null pins with the pot's wiper connected to the minus voltage supply. The op amp is usually shown null adjusted in the open-loop mode, but the extremely high gain of the op amp makes this difficult to achieve. The addition of degenerative feedback aids the nulling process. A sensitive voltmeter or a DC coupled oscilloscope should be used to read the output voltage. Once the output has been adjusted to zero, the op amp can be returned to its operational state, making sure not to change the setting of the potentiometer. The offset voltage adjustment range for the 741 is $\pm 15mV$. This is the range the input offset voltage can be adjusted through the offset nulling pins.

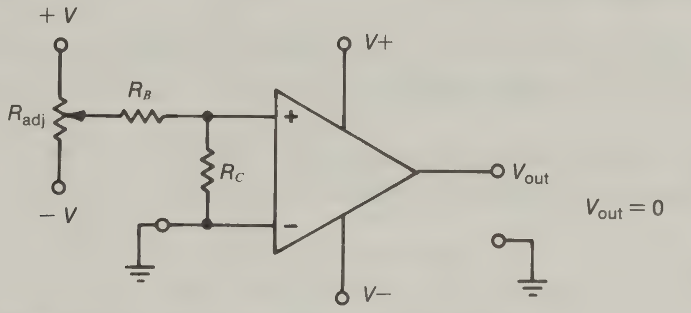


Figure 2-15. An offset voltage compensation network.

For op amps which do not have external null pins, compensating networks must be constructed in one of the input leads, as shown in **Figure 2-15**.

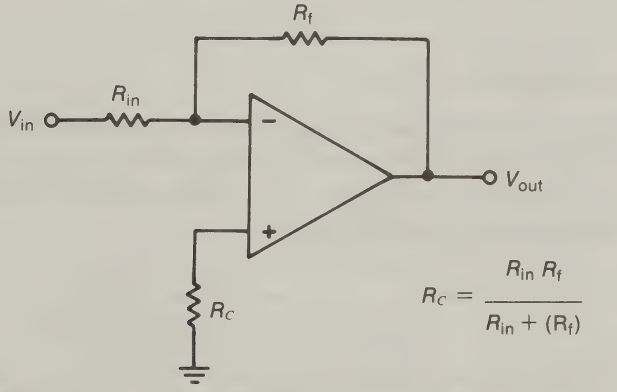


Figure 2-16. Input offset current compensating resistor.

Another inherent condition of the op amp circuit, is the *input offset current*; see **Figure 2-16**. This is the slight difference in bias current flow between the two input pins. The end result of this current imbalance is an output offset voltage. To compensate for this, a resistor (R_c) equal to the parallel value of R_{in} and R_f is inserted in the noninverting input.

$$\text{where: } R_c = \frac{R_{in}\,(R_f)}{R_{in} + R_f} \qquad (2\text{-}25)$$

Topic Review 2-5

1. With the inverting amplifier, ______ was the input impedance of the circuit.
2. In the noninverting amplifier configuration, the input impedance of the circuit, is the input impedance of the ______ ______.
3. Degenerative feedback is still applied to the inverting input to control gain, but V_{in} is applied to the noninverting input; so no ______ ______ occurs.
4. The offset voltage adjustment range for the 741 is $\pm 15mV$. This is the range the input offset voltage can be adjusted through the ______ ______ pins.

Answers:

1. R_{in}
2. op amp
3. phase inversion
4. offset nulling

2-6 Op Amp Power Supplies

Most op amps require dual power supplies (dual voltages) to allow the output to swing positive and negative with respect to ground. Dual supplies can be constructed from two batteries, as shown in **Figure 2-17**. This configuration is limited to short operation, due to depletion of the batteries.

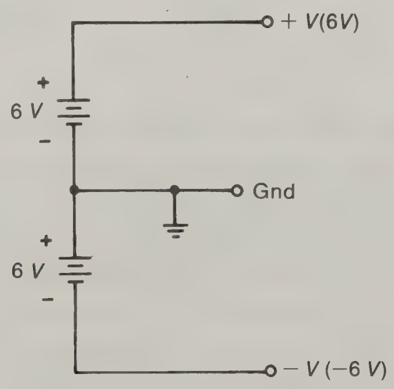


Figure 2-17. Split (dual) supply model.

Some op amps, such as the LM 324, have the capability of operating efficiently with a single supply voltage. Other op amps, such as the 741 family, must have special considerations to allow single supply operations. This is necessary because the 741's input and output voltages are limited as to how near they can be brought to the power supply's voltage levels. The arrangement shown in **Figure 2-18** may be used with most of the circuits discussed in **Chapters 3 and 4**.

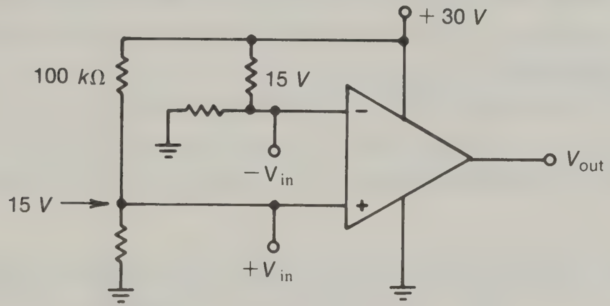


Figure 2-18. Single-supply operations.

A more reliable and popular op amp power supply is the dual-tracking voltage regulator, shown in **Figure 2-19**. These power supplies use IC regulators to provide very stable positive and negative supply voltages.

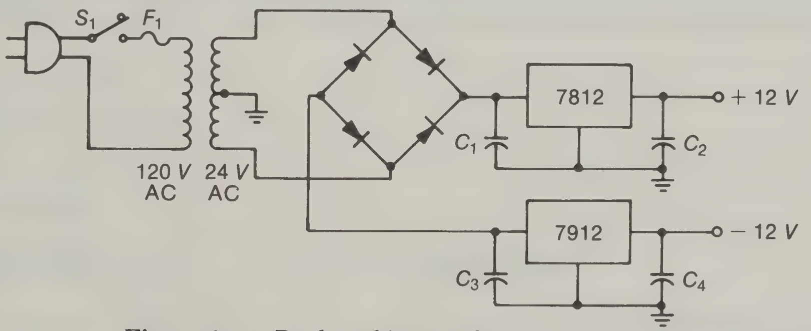


Figure 2-19. Dual-tracking requlator.

The positive (7812) and negative (7912) IC regulators provide guaranteed levels of regulated DC output voltage from the full-wave rectifier bridge. The capacitor network shorts out any high-frequency ripple; capacitor network values are recommended by the manufacturer's data sheets.

The power supply must be capable of supplying the rated supply current of the op amp and any additional current, due to input signals or loads. This is an important consideration with dual-tracking supplies, because the IC regulators come in a limited number of current capabilities. It should also be noted that the input voltage of the regulator must be two volts greater than the desired, regulated output voltage (see three-terminal regulators, **Chapter 9**).

As was previously mentioned, integraged circuits are very susceptible to damage, due to heat. When working with IC's, care must be taken to prevent excessive amounts of current from being drawn from the power supply through the chip. Referring to the data sheet (figure 2-7), the rated supply current shown is the amount of current typically drawn from the power supply by the chip under no load/no input conditions. Also referring to the data sheet, we can find the manufacturer's rated, maximum power dissipation.

When a load is connected to the IC, the load current must be delivered through the chip. This extra current increases the amount of power the chip must dissipate. The total power the chip must dissipate under load can be calculated simply by:

$$P_L = V_L I_L \tag{2-26}$$

When choosing a power supply for a particular application, the minimum current capabilities of the power supply should exceed the maximum current requirements of the IC and the load. By selecting a power supply which provides ten percent more current than the circuit requires, loading of the power supply will be avoided.

The maximum supply voltage listed in the data sheet is only an indication of the maximum power supply voltage the IC can withstand. Extended operation near this value will tend to lessen the performance of the chip severely. Steps should be taken to prevent power supply overvoltage and power supply reversal. **Figure 2-20** shows preventative steps to protect against these destructive conditions. The diode arrangement shown in "Part a" of the figure prevents damage to the op amp from inadvertant supply voltage reversal. The zener diodes in "Part b" of the figure are chosen so that their breakdown voltages are just below the maximum allowable supply voltage of the op amp. Limiting resistors are necessary to limit current flow from the power supply through the zener diodes.

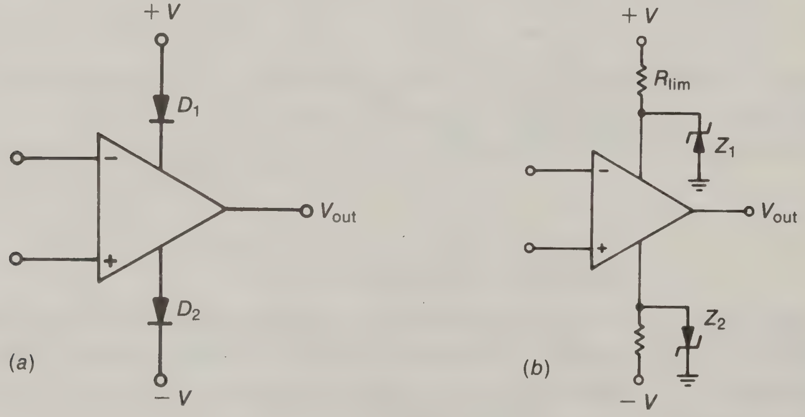


Figure 2-20. Power supply protection circuits.

With the information from the data sheet in hand, we are ready to investigate the many uses of the op amp and other linear integrated circuits.

Topic Review 2-6

1. A more reliable and popular op amp power supply is the _______ _______ voltage regulator.

2. Integrated circuits are very susceptible to damage, due to _______.

3. The _______ _______ _______ is the amount of current typically drawn from the power supply, by the chip, under no load, no input conditions.

4. The _______ _______ _______ listed in the data sheet is only an indication of the maximum power supply voltage the IC can withstand.

Answers:

1. dual-tracking
2. heat
3. rated supply current
4. maximum supply voltage

2-7 Summary Points

1. IC op amps are inexpensive, reliable, and easy to use.

2. Conventional op amps have:
    a) high input impedance
    b) high gain
    c) low output impedance

3. Op amps can be obtained in four general packages: metal cannister, flat-pack, DIP, and mini-DIP.

4. Most op amps operate from split (dual) power supplies.

5. Low output impedance is provided in the 741 op amp by a complementary-symmetry output stage.

6. Common mode rejection ratio (CMRR) is a comparison of how well an amplifier amplifies a differential signal, to how much it amplifies a common mode signal.

7. Op amp packages contain one (single), two (dual), or four (quad) amplifiers.

8. Op amps are building blocks that can be combined with discrete components to produce many different applications.

2-8 Chapter Progress Evaluation

1. Input capacitance for the 741 op amp is typically not greater than

2. Op amps with FET inputs tend to have extremely high values of input impedance such as

3. Typical output impedance of the 741 op amp is

4. In **Figure 2-16**, R_{in} equals 10 $k\Omega$, and R_f equals 5 $k\Omega$. To diminish the effects of input offset, what must be the value of R_C?

5. The 741 has a typical input offset current of approximately

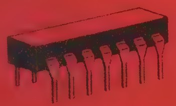
6. If both input bias currents are equal and I_{B_1} equals 20 nanoamps, what is the input bias current?

7. Refer to **Figure 2-4**. When the signal on the noninverting input swings positive

8. Refer to **Figure 2-11**. What is the gain of the op amp if R_f equals 100 $k\Omega$ and R_{in} equals 5 $k\Omega$?

9. If in **Figure 2-11**, the gain is equal to 20 and the input impedance is equal to 10 $k\Omega$, what will be the value of R_f?

10. Refer to **Figure 2-22**. If R_A equals 10 $k\Omega$, and R_f equals 100 $k\Omega$, what must be the value of V_{out} if V_{in} equals 100 millivolts?



Chapter 3

Linear Operations

Objectives

Upon completion of this chapter, you should be able to do the following:

- Explain the operation of summing, averaging, mixing, differencing, and instrumentation amplifiers
- Explain the operation and characteristics of integrators and differentiators
- Explain the theory of operations and applications of precision rectifiers

3-1 Introduction

In this chapter, we will investigate many linear amplifier applications using op amps. Recall that linear applications indicate that the circuit's output will reflect a predictable, proportional representation of the applied input signal. Degenerative feedback is required for these applications.

3-2 Voltage Followers

Voltage followers are circuits which have a gain of one or less, with the output following the input (no phase inversion). Op amps make excellent voltage followers and may be constructed in two forms.

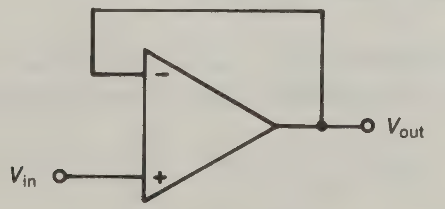


Figure 3-1. Noninverting voltage follower (Buffer).

The noninverting voltage follower, or buffer, shown in **Figure 3-1**, is used as an impedance matching device, because of the op amp's high input impedance and low output impedance. It also provides isolation between circuits.

The performance of the circuit may be analyzed in the same way as the noninverting amplifier.

$$A_v = \frac{R_f}{R_{in}} + 1 \tag{3-1}$$

$$A_v = 0 + 1$$

Therefore: $A_v = 1$

If phase inversion is desired, an inverting amplifier can be constructed as an inverting voltage follower by making R_{in} equal to R_f.

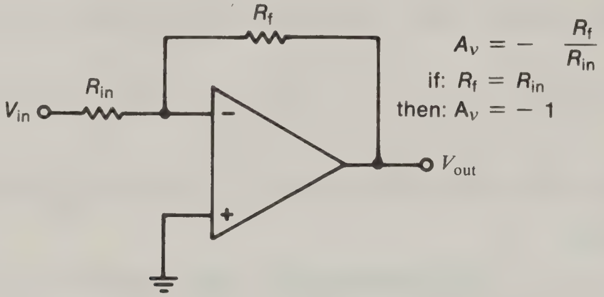


Figure 3-2. Inverting voltage follower

The circuit of **Figure 3-2** has the limitation of a lowered input impedance, due to the zero potential (virtual ground) at the op amp's input created by the feedback loop.

Topic Review 3-2

1. ______ followers are circuits which have a gain of ______ or less, with the output following the input (no phase inversion).

2. The ______ voltage follower, or ______ , is used as an impedance matching device, because of the op amp's high-input impedance and low-output impedance.

Answers:

1. voltage, one
2. noninverting, buffer

3-3 Voltage Summing Amplifiers

The summing amp in **Figure 3-3**, is exactly what its name implies. By adding more input resistors to the basic inverting amplifier, several input signals can be added together. This circuit is also known as an analog adder. Point A is known as the summing point.

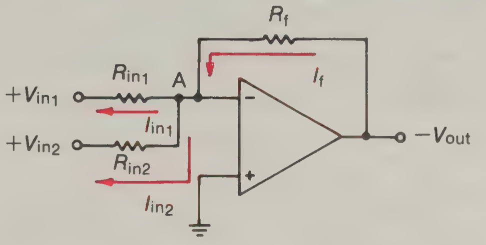


Figure 3-3. Two-input voltage summing amp.

Degenerative feedback holds the op amp's inverting input at virtual ground. This point is referred to as the current summing point. Kirchhoff's current law states that the sum of the currents entering a node equals the sum of the currents leaving a node. Therefore, $I_{R_1} + I_{R_2} = I_{R_f}$ due to the inversion of the output voltage. We can find V_{out}, of **Figure 3-3**, by making the following assumptions and showing that V_{out} is a function of the sum of V_{in_1} plus V_{in_2}:

$$\text{if:} \quad I_1 + I_2 = I_f \tag{3-2}$$

$$\text{and:} \quad I_{R_1} = \frac{V_{in_1}}{R_{in_1}} \tag{3-3}$$

$$\text{and:} \quad I_{R_2} = \frac{V_{in_2}}{R_{in_2}} \tag{3-4}$$

$$\text{and:} \quad I_R = \frac{-V_{out}}{R_f} \tag{3-5}$$

$$\text{then:} \quad I_R = I_{Rin_1} + I_{Rin_2} \tag{3-6}$$

$$\text{and:} \quad \frac{-V_{out}}{R_f} = \frac{V_{in_1}}{R_{in_1}} + \frac{V_{in_2}}{R_{in_2}} \tag{3-7}$$

$$\text{therefore:} \quad V_{out} = -\frac{R_f}{R_{in_1}}(V_{in_1}) + \frac{R_f}{R_{in_2}}(V_{in_2}) \tag{3-8}$$

$$\text{finally, if:} \quad R_{in_1} = R_{in_2} = R_f$$

$$\text{then:} \quad V_{out} = V_{in_1} + V_{in_2} \tag{3-9}$$

Thus, the amplifier output is the sum of V_{in_1} plus V_{in_2}.

The circuit will also subtract negative voltages as in **Figure 3-4**. If one input is positive and the other input is negative, the negative input current will flow toward the summing point. The currents coming into the node must still equal the currents leaving the node, so feedback current (I_f) must be equal to the difference of the two input currents. $I_f = I_{in_1} + (-I_{in_2})$. The input currents, and therefore the input voltages, are independent of each other due to the summing point (virtual ground) at the inverting input of the op amp.

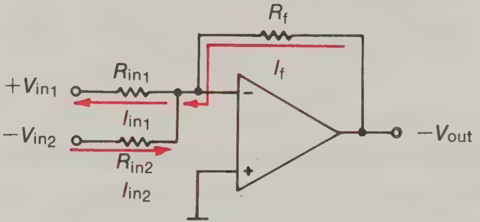


Figure 3-4. Subtracting negative voltages

This configuration can be used with as many input resistors as may be needed. Several variations of the basic summing amplifier are produced by manipulating the values of R_f and the various input resistors. By increasing the value of R_f, the adder can be used with gain. This amounts to multiplying the sum of the input voltages by a constant value.

Also, by using different values of input resistors for the individual inputs, the circuit can be used to add signals with different gains. This amounts to multiplying the individual inputs by different values and is called a *scaling adder*. The circuit can also be used to take the average of a group of input signals. This is accomplished by making all of the input resistors equal to some convenient value (R), while making R_f equal to R divided by the number of inputs. The ability to perform all of these mathematical operations made the operational amplifier indispensable in analog computer operations.

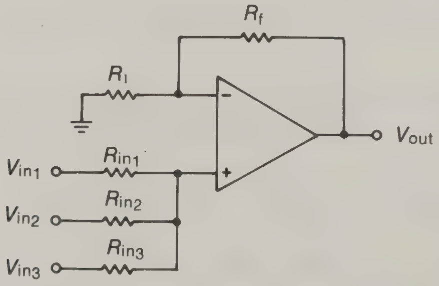


Figure 3-5. A noninverting adder.

A noninverting adder can also be constructed, as shown in **Figure 3-5**. R_1 and all input resistors are made equal to some convenient value. Then, R_f is made equal to $R(N-1)$, where N is the number of inputs. Because of the gain formula for a noninverting amplifier, the output voltage (V_{out}) is simply the sum of the input voltages.

$$A_v = \frac{R_f}{R_1} + 1 \tag{3-10}$$

A summing amplifier with gain may be built by increasing the value of R_f:

Recall:

$$V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \ldots.\right) \tag{3-11}$$

$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 \ldots.\right) \tag{3-12}$$

By making R_f greater than the input resistors, gain is established and V_{out} is equal to the sum of the input voltages times the gain factor. Notice also from the formulas that the gain of any particular input signal is independent of the other inputs.

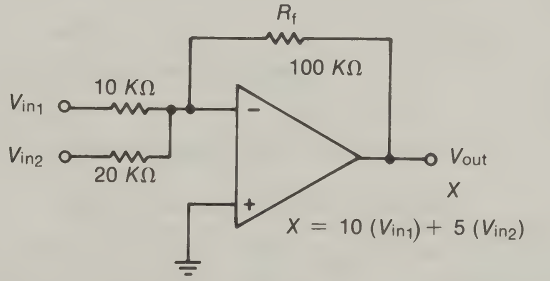


Figure 3-6. A scaling adder performing an algebraic equation.

By allowing the input resistors to have different values, as in **Figure 3-6**, different gains are established for the various inputs. This configuration of the adder is known as a scaling adder and is used when one input should have more effect on the output than another input. This arrangement also allows us to do algebraic equations with the op amp.

Another application of the summing amplifier is in the mixing of audio signals. In this application, shown in **Figure 3-7**, various input signals are taken at different input levels and must be blended to produce a balanced output. Potentiometers are used to adjust the relative volume of their associated input channel, allowing different voice and music channels to be blended to produce a compatible output volume.

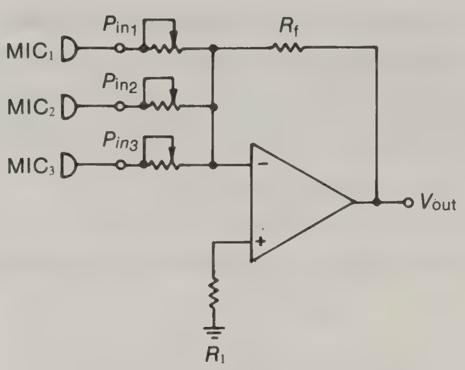

P_{in1}
R_f
MIC₁
P_{in2}
MIC₂
P_{in3}
MIC₃
V_{out}
R_1

Figure 3-7. A three-channel audio mixer

The summing amplifier can also be configured to produce an output that is the average of a set of input signals, as shown in **Figure 3-8**,

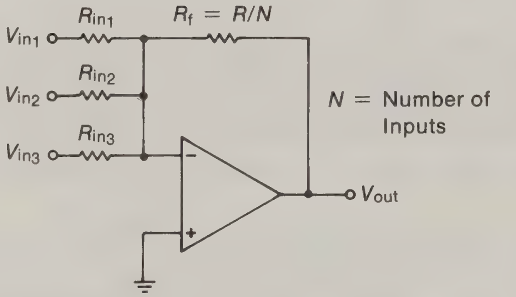

R_{in1}
$R_f = R/N$
V_{in1}
R_{in2}
V_{in2}
N = Number of Inputs
R_{in3}
V_{in3}
V_{out}

Figure 3-8. An averaging amplifier.

$$V_{out} = \frac{V_{in_1} + V_{in_2} + V_{in_3} + \ldots V}{N} \tag{3-13}$$

where N is the number of input channels.

By making R_f equal to the value of the input resistors divided by the number of inputs used, the output voltage will reflect the inverted average of the voltages present at the inputs.

Topic Review 3-3

1. The summing amplifier is also known as a ________ adder.

2. In **Figure 3-3**, point "A" is referred to as the ________ summing point.

3. The summing amplifier will also ________ negative voltages.

4. A summing amplifier with gain may be built by increasing the value of ______.

5. Another application of the summing amplifier is in the ______ of audio signals.

Answers:

1. scaling
2. current
3. subtract
4. R_f
5. mixing

3-4 Differential Amplifier

The differential amplifier utilizes a combination of the inverting and noninverting op amp to produce its output. The output is proportional to the difference between the two input signals, multiplied by the amplifier's gain.

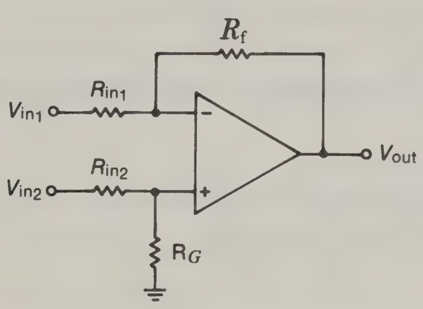


Figure 3-9. Voltage differencing amp

When the output voltage (V_{out}) is due to V_{in_2}, V_{out} is calculated using the voltage established by the divider network ($R_{in_2} - R_G$), multiplied by the gain of the amplifier.

$$V_{out} = V_{in_2} \left(\frac{R_G}{R_{in_2} + R_G}\right)\left(-\frac{R_f}{R_{in_1}} + 1\right) \tag{3-14}$$

When the output voltage (V_{out}) is due to V_{in_1}, V_{out} is calculated using the voltage at the summing point (SP), multiplied by the amplifier's gain.

$$V_{out} = -V_{in} \left(\frac{R_f}{R_{in_1}}\right) \tag{3-15}$$

Total output voltage for the circuit can be calculated by the formula:

$$V_{out} = V_{in_2} \left(\frac{R_G}{R_{in_2} + R_G}\right)\left(\frac{R_f}{R_{in_1}} + 1\right) + \left[-V_{in_1} \left(\frac{R_f}{R_{in_1}}\right)\right] \tag{3-16}$$

By making all the resistors equal, V_{out} can be found simply by:

$$V_{out} = V_{in_2} - V_{in_1} \tag{3-17}$$

The difference amp can also be configured to have gain applied to the difference of the two inputs. By increasing both R_f and R_G in equal amounts, the circuit will produce gain and the output can be calculated by:

$$V_{out} = \frac{R_f}{R_{in_1}} \times (V_{in_2} - V_{in_1}) \tag{3-18}$$

The ratios of R_f/R_{in_1} and R_G/R_{in_2} are usually kept equal. In either case, the output can still be found by the original formula for the difference amplifier.

Beside its application as a mathematical circuit, the differential amplifier is used to suppress common-mode noise signals. They are also commonly used where very small voltages, such as biomedical signals, must be measured or amplified.

Topic Review 3-4

1. The voltage differencing amplifier produces an output that is the ______ between the two inputs.

2. The voltage differencing amplifier is also used to suppress ______-______ noise signals and in cases where very small ______ must be measured or amplified.

Answers:

1. difference
2. common-mode, voltages

3-5 Integrators

An integrator takes the sum of an input signal over the interval of time that the signal is applied. **The circuit's output is a function of the size of the input signal and the amount of time the signal has been applied.**

A capacitor is a natural integrator because the voltage developed across it is dependent on the value of the applied voltage and the RC time constant.

In **Figure 3-10,** a square wave is applied to a basic low pass filter; the capacitor will begin to charge up when the input signal is applied. If the duration of the pulse is long enough, the capacitor will charge up to the applied voltage and level off (saturation). The overall charging cycle of the capacitor is exponential, but if the pulse duration is made much shorter than one RC time constant, the output voltage rise will be more linear in nature.

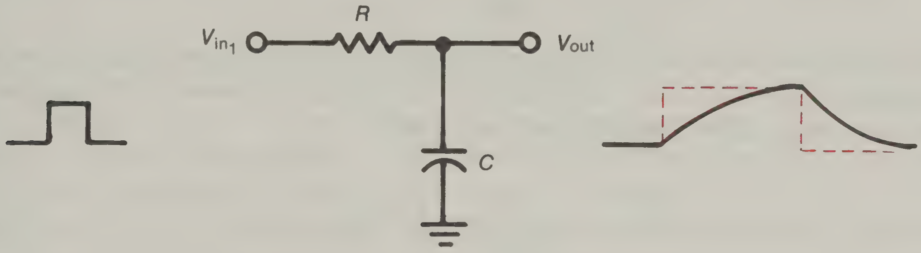


Figure 3-10. Passive low-pass filter integrator

The output of the integrator is only valid as long as the output is not in saturation. When the output is saturated, the output voltage no longer reflects the size and duration of the input signal. A drawback of the passive integrator is that the output voltage is limited to a value less than the input signal, because the input voltage is also distributed between the capacitor and the resistor. This loss of signal is not incurred when an op amp is employed as an integrator. The output can be made equal to or greater than the input.

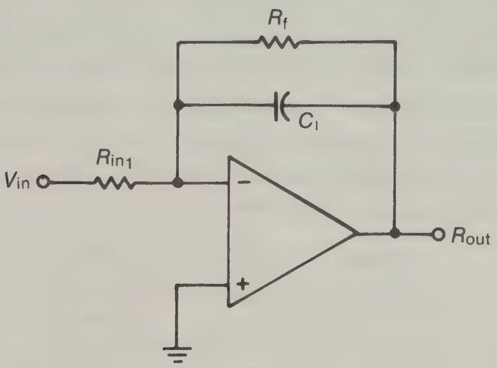


Figure 3-11. An active (op amp) integrator

In **Figure 3-11**, the capacitor is placed in the feedback loop of the op amp, hence, integration of the applied input voltage. Resistor R_f supplies a DC path (offset voltage), to reduce the low frequency gain and therefore improve stability. For frequencies below the cutoff frequency of the integrator, the operating frequency is found by:

$$f_{oper} = \frac{1}{2\pi R_{in_1} C_1} \tag{3-19}$$

Where the integrator acts as an inverting amplifier, the gain is determined by the ratio of:

$$-\frac{R_f}{R_{in_1}} \tag{3-20}$$

Because I_f must equal I_{in}, a constant input voltage will cause constant current to flow through R_{in_1} and C_1. This will cause C_1 to charge up linearly. As long as V_{in} is held constant, V_{out} can be found from this formula:

$$V_{out} = -\frac{1}{R_{in_1}C_1}\,{}_o\!\int^t V_{in}\Delta t \tag{3-21}$$

Recall that the output voltage contains two pieces of information: (1) the size; and (2) the duration of the applied signal. The (−) sign is included in the formula due to the inverting input.

Integrators are designed to integrate a specific frequency. Therefore, a constant is included at the beginning of the formula to account for the design frequency of the integrator.

$$f \qquad \text{where: } R_{in_1}C_f = \text{time}$$

The integral symbol ($\int$) is an old English "S" and is used to indicate that the integral operation is in process, as opposed to the Greek letter (Σ) for statistical summation. O and t are the lower and upper time interval limits of integration. V_{in} is the amplitude of the input voltage. The term Δt represents the change of time during the operation. To integrate a complete square wave, the upper limit of integration and the change of time (Δt) are the same. **Remember that the interval of time of integration is much less than one time constant.**

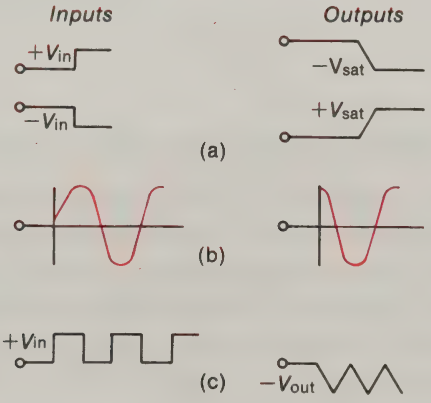


Figure 3-12. Integrator input/output waveforms

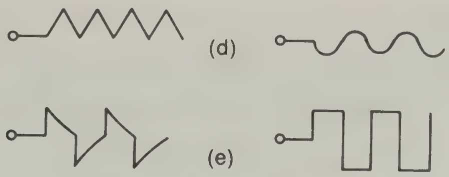


Figure 3-12 (Continued)

When the positive square wave of **Figure 3-12a** is applied to an op amp integrator, the output will ramp downward (−) for the duration of the pulse. If the duration of the pulse is too great or if a constant DC voltage is applied to the input, the output will ramp to saturation and remain there until the input returns to zero. **Figure 3-12** shows some common input waveforms and resulting outputs.

Let's design an integrator to integrate a 1 *kHz* square wave signal. First, the RC time constant must be calculated:

$$t_{(\text{period})} = \frac{1}{f} = \frac{1}{1\ kHz} \tag{3-22}$$

$$t = 1\ msec$$

Next, a value of capacitance for the circuit should be chosen. The capacitor is chosen first because there are many more resistor values to choose from to establish the RC time constant than capacitors. In this case let's choose a 0.1 μF capacitor. The value of the resistor is calculated by rearranging the RC time constant formula:

$$t = RC \tag{3-23}$$

$$\text{so:}\ \ R = \frac{t}{C} \tag{3-24}$$

$$R = \frac{1\ msec}{0.1\ \mu F}$$

$$R = 10\ k\Omega$$

Topic Review 3-5

1. An integrator produces an output signal that is a function of the ______ of the input signal with respect to time.
2. The output of the integrator is only valid as long as the output is not in ______ .

Answers:

1. integral
2. saturation

3-6 Op Amp Differentiator

Differentiation is the reverse operation of integration. A differentiator responds only to changes in input signal. A differentiator is a circuit whose output signal is a derivative of its input waveform. Two of its applications are in analog configuration and wave shaping. As shown in **Figure 3-13**, a passive high-pass filter may be used to perform differentiation.

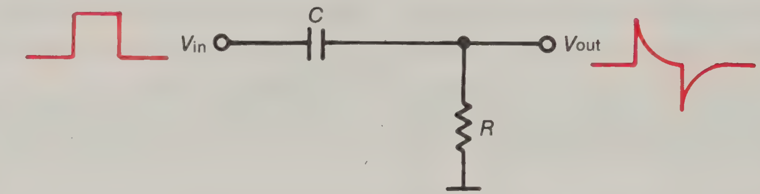


Figure 3-13. Passive high-pass filter differentiator

When an input signal is applied, the entire input voltage will appear initially across the resistor. As the capacitor charges, the voltage across the resistor decreases until the capacitor is fully charged up and cuts off the current flow. Once the capacitor has fully charged, only a change in input will cause an output to appear. The circuit acts as a differentiator only for frequencies *below*:

$$f_{\text{oper}} = \frac{1}{2\pi RC} \tag{3-25}$$

The same limitations associated with the passive integrator are also present with the passive differentiator. An op amp allows the output of the differentiator to have values equal to or greater than V_{in}. An op amp differentiator is shown in **Figure 3-14**.

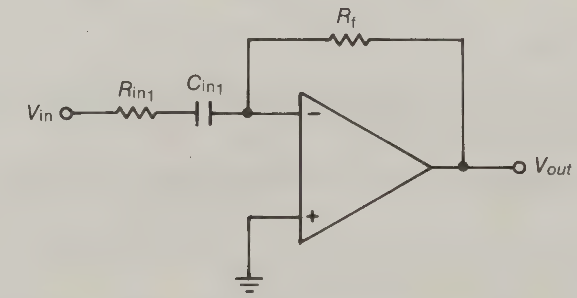


Figure 3-14. An op amp differentiator

The operation of this circuit is the same as the passive differentiator. Once charged, the capacitor will pass only changes in V_{in}, so only changes in input will cause current to flow through R_f. V_{out} will be equal to the voltage across R_f and is proportional to the inverted derivative of the input. V_{out} then, is dependent on the value of V_{in}, the amount of time the input has been present (Δt), and the RC time constant. The formula for determining V_{out} is:

$$V_{\text{out}} = -\, R_f\, C_{\text{in}_1} \frac{\Delta V}{\Delta t} \tag{3-26}$$

when differentiating the positive or negative change of a wave. When differentiating a symmetrical wave, over the entire period of the wave, the formula is:

$$V_{out} = 2\, R_f\, C_{\text{in}_1} \frac{\Delta V}{\Delta t} \tag{3-27}$$

where Δt is equal to the period of the wave.

V_{out} of a square wave is difficult to calculate due to the sharp rise and fall of the input. Since a differentiator acts opposite to an integrator, by differentiating a triangle wave we should get a square wave output. When a ramp function is applied to the input, the current through the capacitor, and therefore through R_f, will remain constant as long as the rate of change of V_{in} is constant. Remember $V_{\text{out}} = V_{Rf}$. When the triangle wave stops ramping (peaks), the capacitor cuts off the current flow and the output drops to zero. As the wave ramps downward, the current through the capacitor reverses direction and the polarity of the output changes.

Resistor R_{in_1} is included to limit the high-frequency (noise) gain of the circuit. For frequencies above

$$f_{\text{oper}} = \frac{1}{2\pi R_{\text{in}_1} C_{in_1}} \tag{3-28}$$

the circuit operates as an inverting amplifier with gain determined by:

$$-\frac{R_f}{R_{\text{in}_1}}$$

As was the case with the integrator, differentiators are designed to differentiate a specific frequency. As an exmaple, let's design a circuit to differentiate a 1 *kHz* signal, with a high frequency gain limited to 10.

The $R_f\, C_{\text{in}_1}$ time constant should be equal to the period of the input signal.

$$t = \frac{1}{1\ kHz} = 1\ msec \tag{3-29}$$

With a 0.1 μF capacitor;

$$\text{if: } t = R_f\, C_{in_1} \tag{3-30}$$

$$\text{then: } 1\ msec = R_f \times 0.1\ \mu F$$

$$\text{so: } R_f = \frac{1\ msec}{0.1\ \mu F} \tag{3-31}$$

$$\text{therefore: } R_f = 10\ k\Omega$$

$$\text{next: } A_v = -\frac{R_f}{R_{in_1}} \tag{3-32}$$

$$\text{then: } 10 = -\frac{10\ k\Omega}{R_{in_1}}$$

$$R_{in_1} - \frac{10\ k\Omega}{10} \tag{3-33}$$

$$\text{therefore: } R_{in_1} = 1\ k\Omega$$

In **Figure 3-15**, the input waveforms were produced by an op amp differentiator.

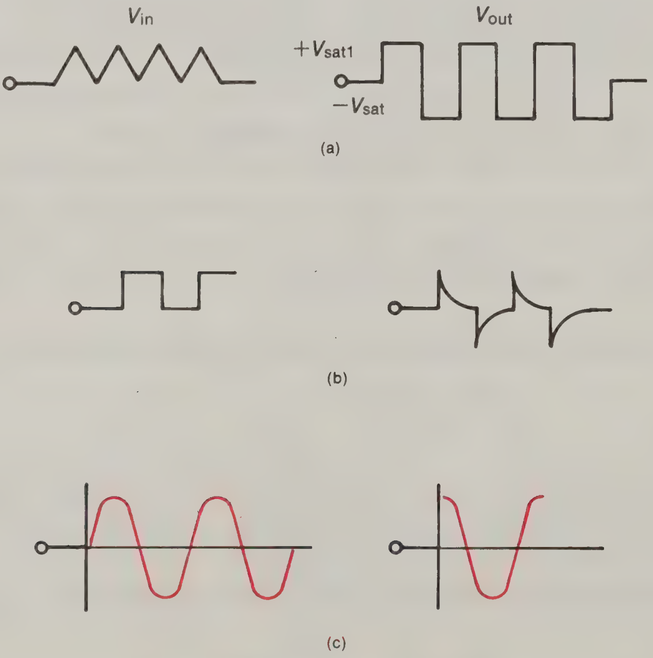


Figure 3-15. Differentiator input/output waveforms

Topic Review 3-6

1. A differentiator is a circuit whose output signal is a ______ of its input.

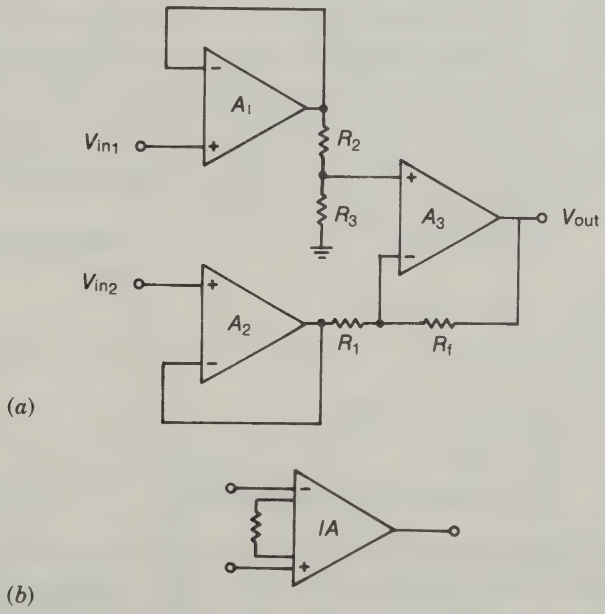
2. Differentiators are designed to differentiate a specific ______ .

Answers:

1. derivative
2. frequency

3-7 Instrumentation Amplifiers

The instrumentation amplifier is a valuable circuit in applications where small signal voltage must be measured precisely. It is used widely in the area of process control, where small signal voltages produced by transducers such as thermocouples, differential pressure sensors, and strain must be measured and amplified. The instrumentation amplifier is also used widely in the biomedical field. In general, the instrumentation amplifier is useful where precise, small signal amplification is necessary.



(a)

(b)

Figure 3-16. Basic instrumentation amplifier and schematic symbol

In **Figure 3-16**, the instrumentation amplifier consists of three op amps and four precision resistors. Upon closer inspection it can be seen that the instrumentation amplifier is a combination of two noninverting buffers and a voltage difference amplifier. The buffers provide extremely high input impedance to the amplifier. This is done to insure that the transducer output is not loaded due to the amplifier. The differential amplifier provides the circuit gain and also very high CMRR (refer to the section on differential amplifiers in chapter 1). Since the input buffers provide no gain, the output formula is simply the output formula of the differential amplifier as long as the recommended resistor ratios are maintained.

$$V_{out} = \left(\frac{R_f}{R_1}\right)(V_{in_1} - V_{in_2}) \tag{3-34}$$

If for some reason these ratios are not maintained, the value of the output can be calculated from the full formula for a voltage differential amp. Notice that only the difference voltage between the amplifiers inputs is amplified, not the absolute values. This is what provides the high common-mode rejection ratio of the circuit and allows the amplifier to amplify very small signals that are hidden in much larger signals.

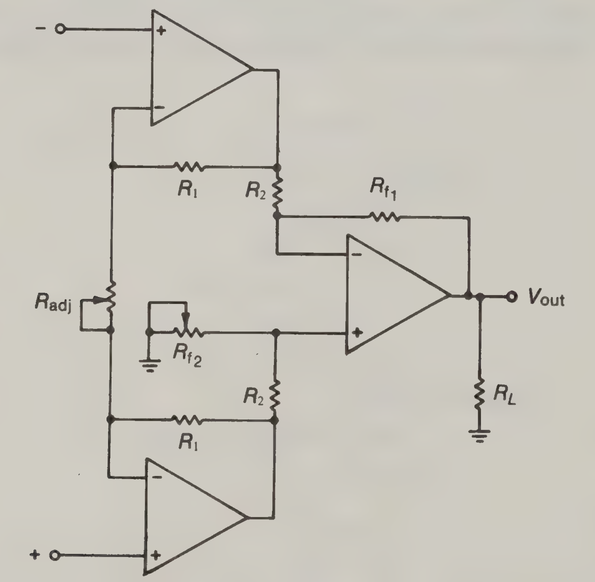


Figure 3-17. Variable gain IA

An adjustable gain instrumentation amplifier configuration is shown in **Figure 3-17**. The gain is adjusted with potentiometer R_{adj}. The circuit's differential input voltage appears across R_{adj}, due to the zero volts differential of the buffers. The potentiometer may be thought of as being in series with both R_1's, so the same current flows through all three. Calculating the gain of the input stage is a simple matter of substituting Ohm's law into the gain formula:

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} \tag{3-35}$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(2R_1 + R_{\text{adj}})(I)}{(R_{\text{adj}})(\text{I})} \tag{3-36}$$

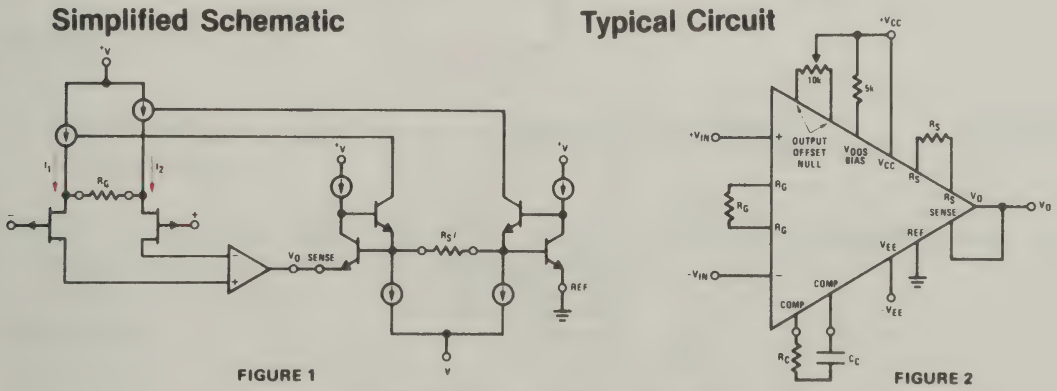
$$A_v = \left(\frac{2R_1}{R_{\text{adj}}} + 1\right) \tag{3-37}$$

Resistor R_f is made variable to allow common mode voltage signals to be balanced out, boosting the CMRR of the circuit. The overall gain of the circuit is determined by the formula:

$$A_v = \frac{R_f}{R_2}\left(\frac{2R_1}{R_{\text{adj}}} + 1\right) \tag{3-38}$$

As can be seen from the formula, increasing the resistance of R_{adj} will result in lower gain and decreasing the value of R_{adj} will give increased gain.

It is possible to obtain good results by constructing instrumentation amplifiers from general purpose op amps if the application requirements are not too rigid, especially when the op amps are in a common package so they are well matched. In this case it is suggested that low power, high slew rate op amps be chosen, along with precision resistors. There are, however, a variety of pre-packaged instrumentation op amps available which provide low offset, drift, and power consumption. These pre-packaged circuits have the drawback of being somewhat expensive. **Figure 3-18** shows the data sheet for an LF152 IC instrumentation amplifier.


Simplified Schematic

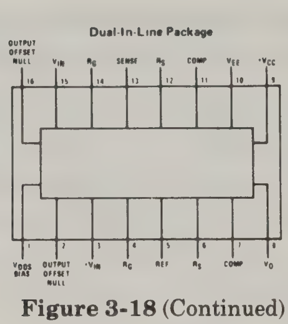
Typical Circuit

FIGURE 1

FIGURE 2

Figure 3-18. LF152 Data sheet
Courtesy National Semiconductor Corp.

Connection Diagram


Dual-In-Line Package
OUTPUT OFFSET NULL
V_IN
R_G
SENSE
R_S
COMP
V_EE
+V_CC
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
V_OOS BIAS
OUTPUT OFFSET NULL
+V_IN
R_G
REF
R_S
COMP
V_O

Order Number LF152D
or LF352D
See NS Package D16C

Figure 3-18 (Continued)

The differential input voltage is applied across resistor R_G which serves the same function as R_{adj} in **Figure 3-17**. In most applications, the sense input is tied to the output terminal to allow the difference between the output voltage and the reference terminal voltage to be felt across resistor R_S, which functions in much the same manner as R_{f_1} in **Figure 3-17**. This allows the gain of the IA to be calculated by:

$$A_v = \frac{R_S}{R_G} \tag{3-39}$$

An internal feedback loop is built into the chip which allows unity-gain operation without external feedback circuitry.

Due to the LF152's two-stage construction, there are two types of offset voltage to be taken into account; the input offset voltage (V_{IOS}) and the output offset voltage (V_{OOS}). The input offset V_{IOS} voltage is produced in the input stage of the IA and will be multiplied by the gain of the amplifier. **Figure 3-19** shows a simple method of nulling V_{IOS} through the compensation inputs.

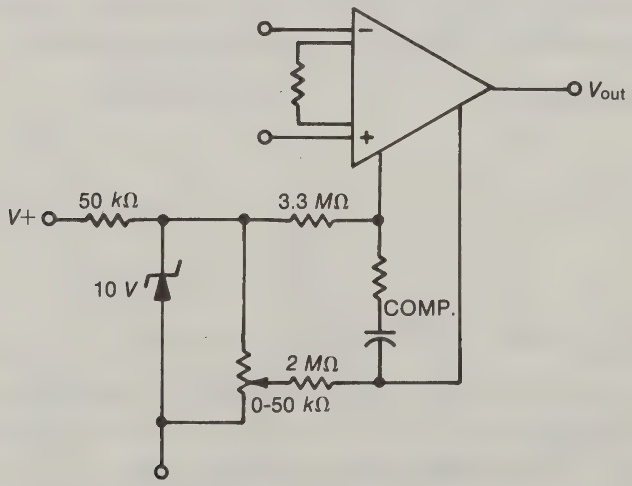

–
+
V_out
V+
50 kΩ
3.3 MΩ
10 V
COMP.
2 MΩ
0-50 kΩ

Figure 3-19. Simple input offset nulling arrangement

On the other hand, the output offset voltage, V_{OOS} is a product of the output stage and is independent of gain. Output offset is nulled through the output offset null pins included on the chip, as shown in **Figure 3-20**.

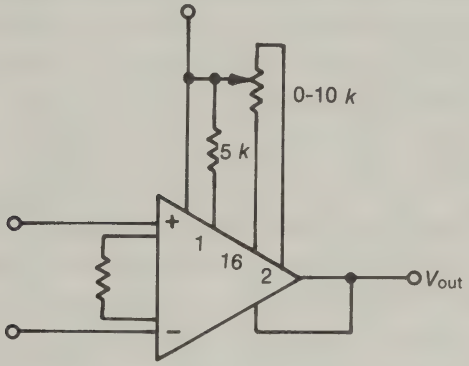


Figure 3-20. Output offset nulling

The total offset of the circuit is expressed as the sum of the two independent offsets:

$$V_{OS} = V_{IOS}(A_v) + V_{OOS} \tag{3-40}$$

If no output offset adjustment is used, pins 1, 2 and 16 must be tied to V+. The reference pin allows the output voltage to be biased to any desired level between +10 and −10 V. For most applications, the sense input is tied to the output. The manufacturer provides the separate sense terminal to allow the LF152 to be used in a variety of specialized applications.

Topic Review - 3-7

1. Instrumentation amplifiers are used where a small signal ______ must be measured precisely.

2. IA's also provide high ______ and allow the amplifier to amplify very small signals that are hidden in much larger signals.

Answers:

1. voltage
2. CMRR

3-8 IA Applications

Instrumentation amplifiers are often used in conjunction with transducer bridges. IA's are ideal for amplifying the small signals developed by these bridge circuits, without loading the bridge. One such bridge circuit is the strain gage bridge shown in **Figure 3-21**.

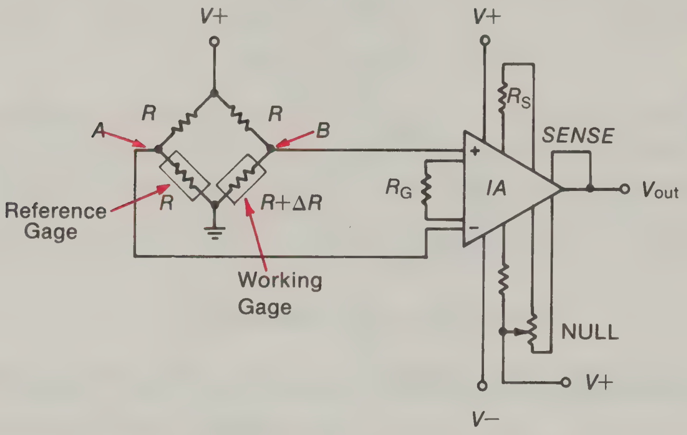


Figure 3-21. Strain gage amplifier configuration

A strain gage is a device used to measure changes in physical pressures. The gage is actually an alloy wire or foil which is bonded to a supporting structure. As force is applied to the structure, the length of the structure and the strain gage will change slightly. This in turn causes the resistance of the gage to change. If the structure is compressed, the resistance of the wire will decrease and if the wire is stretched, its resistance will increase. The resistance change (ΔR) of the wire is directly proportional to its change in length, which is normally in millionths of an inch.

In the bridge circuit of **Figure 3-21**, two strain gages are shown; one, (R + ΔR), is used for the pressure or force measurement and the other, (R), is used as a temperature reference to offset any change in resistance due to temperature change. Manufacturers produce standard strain gages having the compensation gage included in the package, so that both are subject to identical temperatures.

Equal precision resistors are used in the upper legs of the bridge, so that when no force is applied to the measuring wire, the bridge will be balanced and no difference of potential will be present between points "A" and "B." When the wire is compressed, its resistance decreases causing point "A" to become more positive than point "B." When tension is applied to the wire, its resistance decreases and point "B" becomes more positive than "A."

The difference of potential developed between points "A" and "B" is applied to a pre-packaged IA which amplifies the difference voltage and provides a more desirable level of output voltage. The gain of the IA is determined by the ratio of R_S to R_G. A nulling resistor is used to correct any imbalances in the bridge circuit when no forces are applied to the strain wire.

Instrumentation amplifiers can also be used as thermocouple amplifiers. A thermocouple is simply a pair of dissimilar conductors so joined at two points that an electromotive force is developed by the thermoelectric effects when the junctions are at different temperatures. Certain metal combinations have become standards for thermocouples. They produce a very dependable output voltage (generally in the millivolt range) for a given junction temperature.

The point at which the thermocouple is connected to the measuring device is known as the *cold* junction. In practice, it represents another thermocouple, due to the difference between the thermocouple material and the input material of the measuring device. In order to obtain accurate temperature measurements, the measuring circuit must be compensated for the voltage developed by the cold junction temperature.

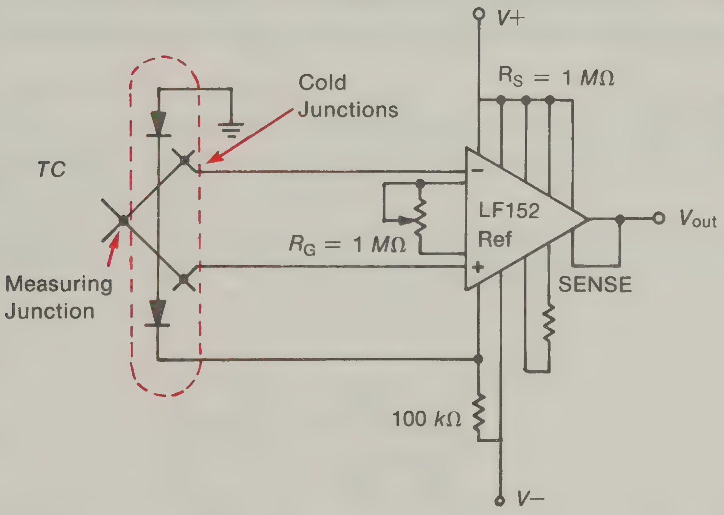


Figure 3-22. Thermocouple amplifier with cold junction compensation

Figure 3-22 shows an LF152 IA configured as a thermocouple amplifier with cold junction compensation. The output voltage for this configuration is determined by:

$$V_{out} = (V+) - (V-)\ \frac{R_S}{R_G} + V_{ref} \tag{3-41}$$

Resistor R_G is adjusted to calibrate the output voltage to some predetermined level, corresponding to the temperature present at the measuring junction of the thermocouple. This calibration adjustment removes the cold junction voltage from the output voltage. Once the circuit is adjusted, two diodes which are mounted in thermal contact with the cold junctions compensate for any change in ambient temperature.

As the measured temperature increases, the thermocouple will produce a greater difference of potential. Only changes in ambient temperature will cause a change of voltage, due to the cold junction.

3-9 Precision Rectifiers

When rectifying small signals, the voltage needed to forward bias diodes can make them ineffective. However, when op amps are used with silicon diodes, circuits can be constructed to precisely rectify even very small signals.

When a positive pulse is applied to **Figure 3-23a**, the op amp will invert the pulse, causing D_2 to conduct, feeding the output back to the input and canceling the input signal. When a negative pulse is applied, the inverted output will cause D_1 to conduct. If $R_f = R_{in}$ the output will be rectified and have a gain of -1. By reversing the diodes (Figure 3-23B) the rectified output polarity can be reversed.

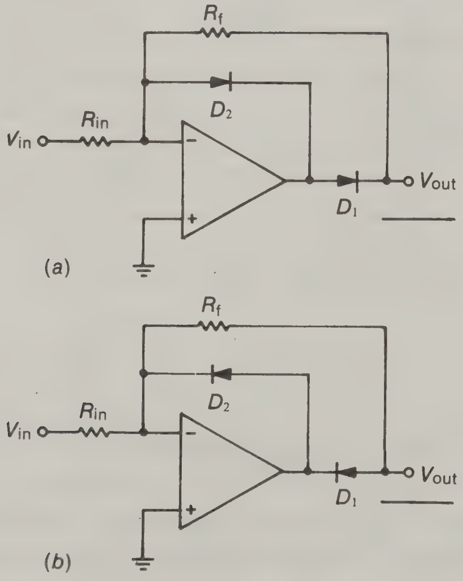


Figure 3-23. Half-wave precision rectifiers

Full-wave precision rectification can be accomplished by combining an inverting and a noninverting half-wave rectifier, as shown in **Figure 3-24**.

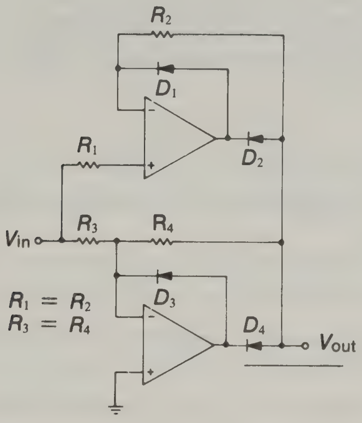


Figure 3-24. Full-wave precision rectification

When a positive pulse is applied to V_{in}, the output of op amp #1 will follow the input, because op amp #1 is configured as a noninverting voltage follower. The op amp output polarity will cause D_1 to conduct while cutting off D_2. Op amp #2 will invert the signal and cause D_4 to conduct. This inverted signal is applied to the output.

When the negative pulse is applied to V_{in}, op amp #1 will produce a negative pulse, causing D_2 to conduct, applying the negative pulse to V_{out}. Op amp #2 will invert the signal causing D_3 to conduct, canceling the input. By reversing all of the diodes the output polarity will be reversed.

Full-wave precision rectification can also be accomplished with a precision, half-wave rectifier and a scaling adder as shown in **Figure 3-25**.

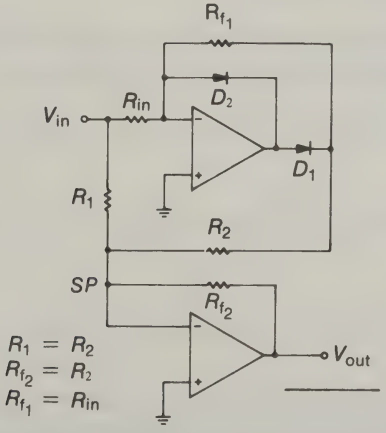


Figure 3-25. Full-wave rectification with a summing amplifier

When the negative cycle of V_{in} is applied, op amp #1 will invert the signal and D_1 will conduct. This negative cycle is also fed to the summing point through R_2. Current flow into SP through R_1 will be twice the current through R_2 because:

$$R_1 = \frac{1}{2} R_2 \tag{3-42}$$

Also, remembering the currents are 180° apart, SP will be positive, but equal in amplitude to V_{in} because:

$$I_{SP} = I_{R_1} - I_{R_2} \tag{3-43}$$

So, V_{out} will be negative as shown in **Figure 3-25** because of the inverted gain of op amp #2.

During the positive cycle of V_{in}, op amp #1 will invert the signal and D_2 will conduct. This results in no output through R_1 because the rectified output is fed back to the input. However, the positive cycle is applied to the SP through R_2, and once again, this provides a negative pulse at V_{out}. This gives the desired full-wave rectification.

Topic Review 3-9

1. In **Figure 3-23a**, applying a positive voltage to the op amp input will cause ______ to conduct. This is because the op amp ______ the input voltage.
2. Full-wave precision rectification can be accomplished by combining an ______ and a noninverting half-wave rectifier.
3. Full-wave precision rectification can also be accomplished by combining a precision ______-______ rectifier with a ______ ______.

Answers:

1. D_1, inverts
2. inverting
3. half-wave, scaling adder

3-10 Summary Points

1. Linear op amp configurations can be used to perform analog math functions such as addition, subtraction, multiplication, averaging integration, and differentiation.

2. The summing amplifier can be used to take the algebraic sum of a virtually endless number of input signals. Variations of this circuit are also used as audio mixers and signal averagers, and can be constructed in both inverting and noninverting form.

3. An op amp differencing amplifier algebraically subtracts the voltage present at the inverting terminal from the voltage level present at the noninverting input.

4. An improved form of the differencing amp is the instrumentation amplifier, which is used to precisely measure and amplify very small input signals.

5. IA's have the advantages of extremely high-input impedance and separately adjustable input and output offset nulling.

6. Integrators sum up an input signal over a period of time, and produce an output that represents the magnitude of the input signal and the amount of time that signal has been applied. An important use of the integrator is as a wave shaping or wave form altering circuit.

7. The differentiator is a circuit which responds only to changes in input voltage.

8. Op amps are very useful in small signal and precision rectification, because the op amp replaces signal losses due to forward biasing the signal path diodes.

9. Full-wave rectification requires two op amp circuits: an inverting and a noninverting half-wave rectifier or a precision half-wave rectifier and a scaling adder.

3-11 Chapter Progress Evaluation

1. If, in **Figure 3-3**, V_{in_1} equals 10 mV and if V_{in_2} equals 20 mV, what is the value of V_{out}?

2. If, in **Figure 3-5**, R equals 10 $k$ohms and there are four inputs, what is the value of R_f?

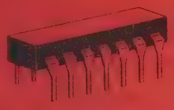
3. What is the algebraic equation to determine V_{out} in **Figure 3-6** if R_{in_1} equals 5 k ohms and R_{in_2} equals 30 $k$ohms?

4. If all resistors are equal in **Figure 3-9**, and V_{in_1} equals 10 mV while V_{in_2} equals 20 mV, what is the value of V_{out}?

5. What is the operatig frequency, f_{oper}, of the integrator of **Figure 3-11 when** R_{in_1} equals 10 *k*ohms and C_1 equals 0.01 μF?

6. What is the time, in milliseconds, of integration of a 1*MHz* square wave?

7. In **Figure 3-17**, R_{adj} equals 1 *k*ohm, R_1 equals 1 *k*ohm. What is the gain, A_v, of the IA?



Chapter 4

Comparators

Objectives

Upon completion of this chapter, you should be able to do the following:

- Explain the operation of voltage comparators
- Describe the operation of zero crossing, or level detectors
- Describe the operation of phase-shift detectors
- Describe the theory of operation behind multiple-level indicators and their applications

4-1 Introduction

The simplest operational amplifier circuits are *comparators*. These circuits use one input to the op amp as a reference to which the other input is compared. Op amp comparator operations provide nonlinear output responses. Because of the extremely high gain of the op amp, any difference between the inputs greater than approximately 55μ volts will drive the output to plus or minus saturation, depending upon the relative polarities of the inputs.

A simple comparator compares the voltage level of one input to the voltage level of the other input. Input voltage levels may also be compared to zero (ground), or some fixed positive or negative voltage reference. The output condition for a given input condition is dependent upon which input (+ or −) is used as the reference.

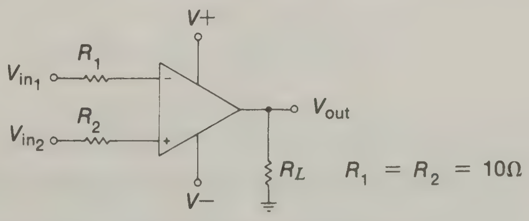


Figure 4-1. A simple voltage comparator

In **Figure 4-1**, the differential amplifier inside the op amp detects the difference between the two input signals (V_{in_1} and V_{in_2}). The output voltage is determined by which input signal is the more positive of the two. If V_{in_1} is more positive than V_{in_2}, the inverting side of the differential amplifier is in control and the output is driven to negative saturation. When V_{in_2} becomes more positive than V_{in_1}, the noninverting side of the diff amp is in control and the output swings to positive saturation. **This relationship is true, even if both values of input voltage are negative.**

Equal values of input resistance should be used to minimize input offset currents.

Comparators are used widely in digital applications which tend to operate at very high frequencies. Op amps with frequency compensation have reduced slew rates. To allow the op amp's output to switch from one saturation level to the other rapidly, the use of uncompensated op amps may be necessary.

Topic Review 4-1

1. In a simple voltage comparator, the output voltage is determined by the more ______ of the two input signals.
2. This relationship is true, even if both values of input voltage are ______.
3. Equal values of ______ ______ should be used to minimize input offset currents.

Answers:

1. positive
2. negative
3. input resistance

4-2 Zero Crossing Detectors

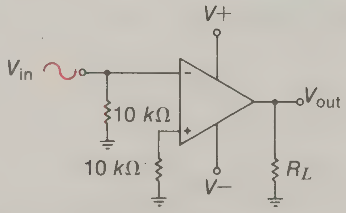


Figure 4-2a. An inverting zero crossing detector

In **Figure 4-2a**, the output changes state each time the input signal crosses ground (from positive to negative or negative to positive).

The inverting *zero crossing detector* utilizes the op amp's noninverting input as the reference which is tied to ground. The input signal is applied to the inverting input. As long as the input signal is positive, the inverting input is the more positive input and the output is at negative saturation. When the input dips negative on the half cycle, the noninverting input becomes the more positive input and the output swings to positive saturation.

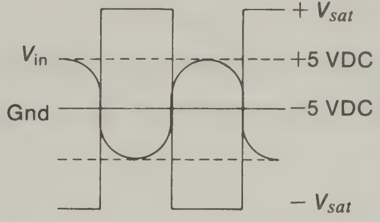


Figure 4-2b. Input/Output relationship

In **Figure 4-2b**, the output swings from negative to positive saturation, 180° out of phase with the input signal.

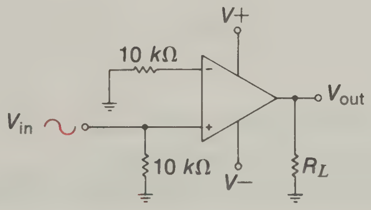


Figure 4-3a A noninverting zero crossing detector

In **Figure 4-3a**, the principle of operation is the same for the noninverting zero crossing detector as it was for the inverting configuration (figure 4-2A). The only difference is that the inverting input is now the ground reference, and the input signal is applied to the noninverting input.

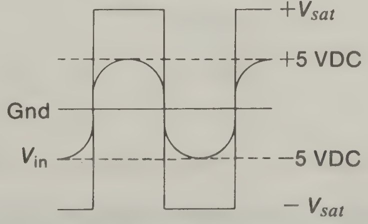


Figure 4-3b. Input/Output relationship

In **Figure 4-3b**, the output swings from positive to negative saturation, in phase with the input signal.

These two circuits are used as sine-to-square-wave converters.

Topic Review 4-2

1. In zero crossing detectors, the ______ will change state each time the ______ ______ crosses ground.
2. In the inverting zero crossing detector, the op amp's ______ input is used as a reference and is tied to ______.
3. In the noninverting zero crossing detector, the op amp's ______ input is used as a reference and is tied to ______.

Answers:

1. output
   input signal
2. noninverting
   ground
3. inverting
   ground

4-3 Phase Shift Detectors

Op amp comparators are also used to detect the phase difference between two input signals.

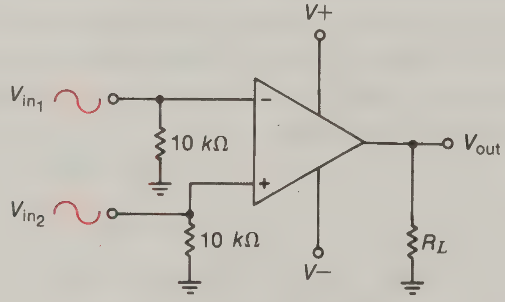


Figure 4-4a. Phase difference detector

As in **Figure 4-4a**, when the input signals are in phase, the output voltage should be near zero, due to common mode rejection. As the inputs become out of phase, the output voltage changes from positive to negative saturation at the point in time when V_{in_1} becomes more positive than V_{in_2}. This is because V_{in_1} is the inverting input.

Likewise, the output changes from negative to positive when V_{in_2} becomes more positive, since V_{in_2} is the noninverting input. This is shown in **Figure 4-4b**.

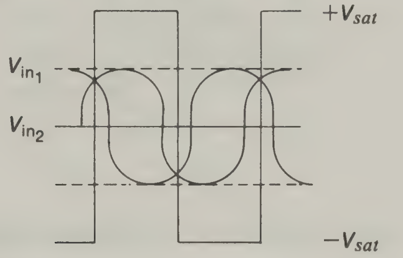


Figure 4-4b. Input/Output relationship

Topic Review 4-3

1. Op amp comparators may also be used to detect ______ ______ between two input signals.

2. When the two ______ signals are in phase, the output voltage should be near zero, due to common mode rejection.

3. As the input voltages become out of phase with each other, the ______ ______ will change from ______ to ______ saturation at the point in time when the inverting input becomes more positive than the noninverting input.

Answers:

1. phase difference
2. input
3. output voltage
   positive
   negative

4-4 Voltage Level Detectors

Comparators are also used to detect voltage levels other than zero (ground). These are called *voltage level detectors* (see figure 4-5). A fixed detection level or reference voltage is established by a resistive voltage divider from $V+$ to ground. The reference voltage is applied to the inverting input, and the input signal is applied to the noninverting input.

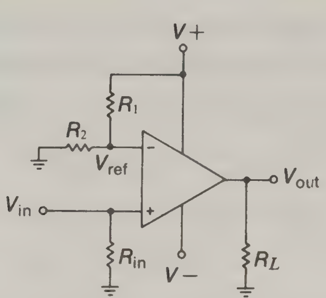


Figure 4-5. Positive voltage level detector

When the signal voltage becomes more positive than the reference voltage, the op amp's output voltage goes to positive saturation. Anytime the signal is below the reference voltage, the output voltage is at negative saturation.

To establish the resistive voltage divider, and therefore the reference voltage, the general voltage divider formula is used.

$$V_{ref} = \frac{R_2}{R_1 + R_2}(V+) \tag{4-1}$$

It is good practice to use equivalent input resistors with op amp comparators, so resistor R_2 should be chosen to equal the other input resistor R_{in}, (values from 1 $k\Omega$ to 50 $k\Omega$ generally make good choices for the resistor voltage divider).

In reference to **Figure 4-5**, let's design a level detector to detect +3.7 volts. Since we have used 10 $k\Omega$ input resistors up to this point, let's assume a value of 10 $k\Omega$ for R_2. Also, assuming a supply voltage of +12 volts, we can solve the general voltage divider formula for an appropriate value of R_1.

$$V_{ref} = \frac{R_2}{R_1 + R_2}(V+)$$

Substituting:

$$3.7V = \frac{10\ k\Omega}{10k\Omega + R_1}(12V)$$

$$3.7V = \frac{(10k\Omega)(12V)}{10k\Omega + R_1}$$

$$(3.7)(10k + R_1) = (10k)(12)$$

$$3.7\ R_1 + 37k = 120k$$

$$3.7\ R_1 = 120k - 37k = 83k$$

$$R_1 = \frac{83\ k}{3.7}$$

Therefore:

$$R_1 = 22\ k\Omega$$

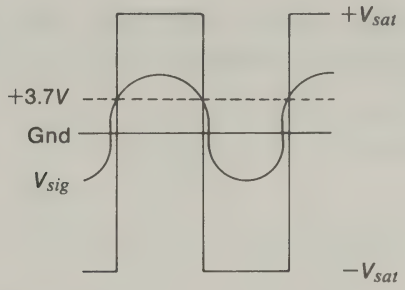


Figure 4-6. Input/Output relationship

In **Figure 4-6**, as the input voltage swings from negative to +3.7 volts, the op amp output voltage goes to positive saturation or $+V_{sat}$.

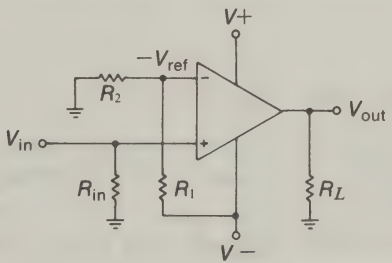


Figure 4-7. Negative voltage level detector

As in **Figure 4-7**, negative voltage level detectors can also be constructed by running the resistive voltage divider from minus supply to ground.

Voltage level detectors can also be built with the inverting input as the signal sensing input and the reference voltage as the noninverting input. The output voltage simply swings in the opposite direction from what was previously stated.

Topic Review 4-4

1. Comparators can be used to detect voltage levels other than ______ or ______ volts.
2. A fixed detection level or ______ voltage is established by a resistive voltage divider from $V+$ to ground.
3. For positive voltage level detectors, the reference voltage is applied to the ______ input and the input signal is applied to the ______ input.
4. Voltage level detectors are also constructed by running the resistive voltage divider from the ______ supply to ______.

5. Voltage level detectors can also be built with the ______ input as the signal sensing input and the reference voltage on the ______ input.

Answers:

1. ground or zero
2. reference
3. inverting
   noninverting
4. negative
   ground
5. inverting
   noninverting

4-5 Voltage Window Detectors

A *voltage window detector* circuit monitors an input signal and indicates when the signal is either (**a**) outside of preset limit conditions or (**b**) when the signal is operating within its limits, depending upon the circuit configuration. **The predetermined limits "frame" the upper and lower limit voltages, hence the name *voltage window detector.***

Many digital circuits must have closely regulated supply voltages to operate properly. TTL (transistor - transistor logic) circuits operate at +5 volts DC. The absolute limits of operating voltage for these circuits range from +5.5 volts to +4.5 volts, so their power supplies must be regulated within this range or window.

A window detector configured to monitor a TTL power supply voltage, and indicate an alarm condition whenever the voltage is outside the window, is shown in **Figure 4-8**.

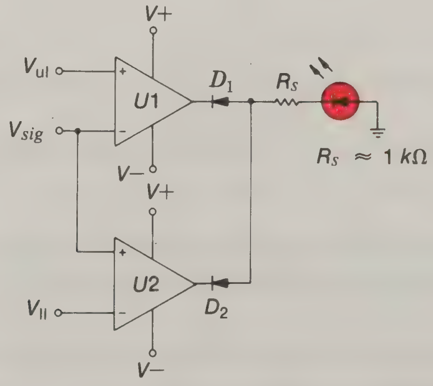


Figure 4-8. Voltage window detector, outside limits

Anytime the input voltage is within the window, both op amps are at positive saturation and the LED is prevented from lighting. If the signal voltage becomes greater than the upper limit reference voltage (V_{ll}), op amp #1's output swings to negative saturation ($-V_{sat}$), allowing current to flow through D_1, lighting the LED. Likewise, if the signal voltage falls below the lower voltage limit (V_{ll}), the output of op amp #2 goes to $-V_{sat}$ and the LED will light.

Diodes D_1 and D_2 are included to prevent interaction between the op amp outputs. Resistor R_S is a current limiting resistor for the LED, and may be lower in value than the one stated or omitted completely. This depends on the value of V_{out} and current limitations of the op amp used.

Two separate LED's may be used to construct a high/low alarm indicator, as shown in **Figure 4-9**. A dual op amp chip makes these circuits inexpensive to use.

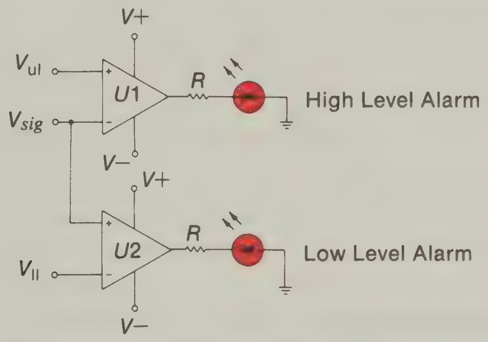


Figure 4-9. High/Low level alarm

By configuring the comparators as in **Figure 4-10**, the window detector can be used to indicate when the signal is within the window.

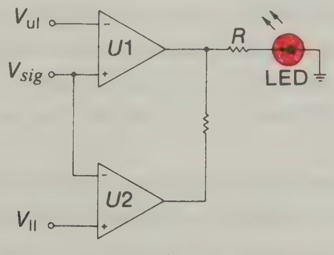


Figure 4-10. Voltage window detector

When the signal voltage is within the window, the outputs of both op amps are at $-V_{sat}$, which causes the LED to light. If the input signal goes above or below the window limits, the affected op amp's output swings to $+V_{sat}$, and the two outputs cancel each other (providing the op amps + and − saturation levels are within approximately 1.6 volts of each other). The LED will then go out.

NOTE: The op amps may need to be null adjusted for this application.

Topic Review 4-5

1. A voltage window detector circuit monitors an ______ signal and can indicate when the signal is within or outside preset voltage limits.

2. The window detector circuit uses ______ comparators with the input signal applied to the ______ input of one comparator and the ______ input of the other.

3. Voltage window detectors are often used to monitor a ______ ______ voltage and indicate an alarm condition whenever that voltage is outside of its preset upper or lower limits.

Answers:

1. input
2. two
   inverting
   noninverting
3. power supply

4-6 Multiple Level Indicators

A popular application of op amp comparators is the implementation of multiple level displays. This application is being used increasingly in audio equipment, medical equipment, automobiles, and analog meter displays. These comparator circuits usually consist of little more than a calibrated voltage divider, op amp comparators, and multiple colors of LED's. The result is informational displays that can be read at a glance, or even at a distance. These displays can be constructed to indicate either linear or logarithmic scales.

Figure 4-11 illustrates a five-level fuel-level indicator for an automobile.

A standard gas tank float assembly is shown inside the dotted lines of the figure. When the tank is full, the float assembly (rheostat) shorts the resistive element to ground, and V_{level} is zero. As the level in the tank diminishes, the resistive element of the rheostat decreases, increasing V_{ref}.

V_{ref} is also applied to an equal value resistive voltage divider, which establishes individual reference voltages at the noninverting inputs of the comparators. As the level in the tank decreases, the voltage at V_{level} increases. As V_{level} becomes greater than the individual reference voltages, the inverting inputs of the op amps cause their outputs to go to ground and turn off the individual LED's.

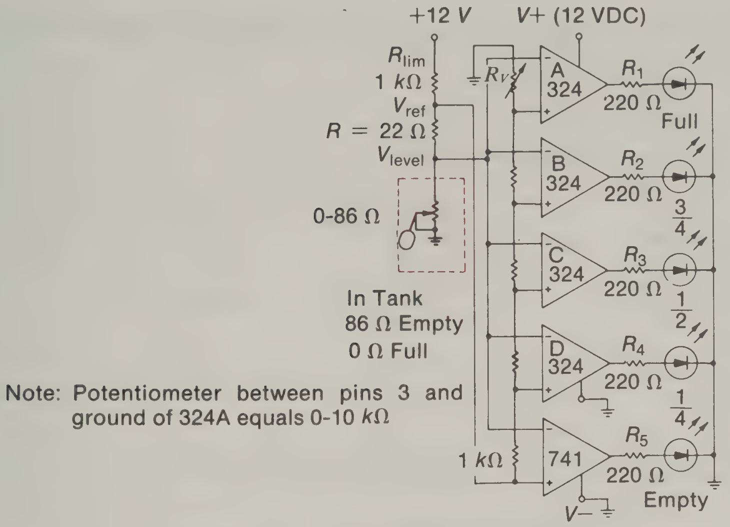

+12 V
V+ (12 VDC)
R_{lim}
1 kΩ
V_{ref}
R = 22 Ω
V_{level}
0-86 Ω
In Tank
86 Ω Empty
0 Ω Full
Note: Potentiometer between pins 3 and ground of 324A equals 0-10 kΩ
R_V
A
324
B
324
C
324
D
324
741
1 kΩ
V−
R_1
220 Ω
Full
R_2
220 Ω
3/4
R_3
220 Ω
1/2
R_4
220 Ω
1/4
R_5
220 Ω
Empty

Figure 4-11. Five-level fuel gauge

Resistor R_{lim} is incorporated to limit current through the sensing element. The rheostat (R_V) at the end of the voltage divider leg allows the level indicator to be easily calibrated. The current limiting resistors for the LED's may be omitted if the op amps have current limited outputs.

This configuration may be expanded to indicate as many levels as desired. Similar configurations are used to provide voltmeter displays, oil pressure gauges, and many other applications. The popularity of these configurations has prompted IC manufacturers to produce pre-packaged versions of these circuits. The LM 3914, 3915, and 3916 bar graph/dot display drivers are examples.

From **Figure 4-12**, it can be seen that the operation of the LM 3914 is identical to the discrete op amp voltage divider, shown in **Figure 4-11**.

The internal voltage divider establishes ten equally divided reference voltages for the ten op amp comparators. As the input voltage increases, exceeding the individual reference voltages, the comparator outputs go low, turning on the LED's in equal steps. The input signal is applied to an op amp buffer, which provides high input impedance for the chip. The input is also protected against reverse polarity signals by a clamping diode.

An internal user programmable voltage reference is included to provide a constant current reference, regardless of supply voltage and load variations. The mode select pin is used to control the style operation, and to allow cascading of multiple 3914's. Tying the mode select pin to $V+$ provides a bar graph output display. Tying to $V-$, or leaving the pin open, gives a dot display operation

The 3914 can be used to drive LED's, LCD's, external drive transistors, vacuum fluorescent lamps, and can be cascaded to produce displays of up to 100 elements.

The display driver can be used with a wide range of supply voltages (3-25 Volts) and is highly tolerant of fluctuating supplies.

Block Diagram (Showing Simplest Application)

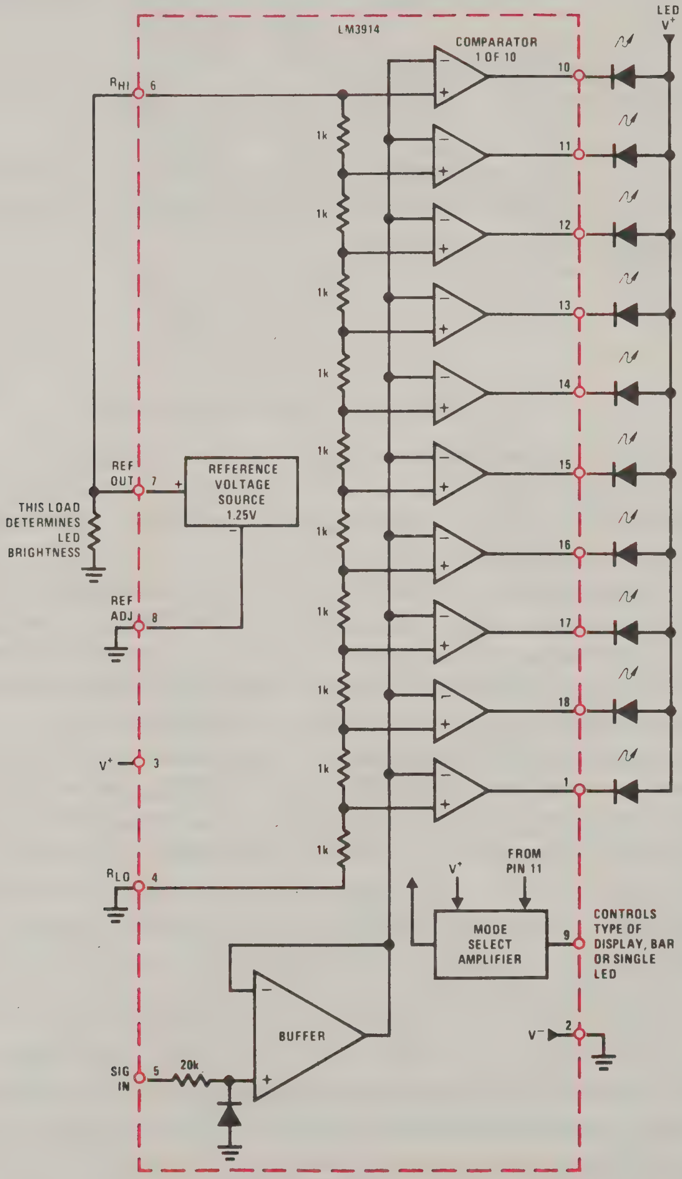

LM3914
LED V+
COMPARATOR 1 OF 10
R_HI 6
1k
10
11
12
13
14
15
16
17
18
1
REF OUT 7
REFERENCE VOLTAGE SOURCE 1.25V
THIS LOAD DETERMINES LED BRIGHTNESS
REF ADJ 8
V+ 3
R_LO 4
V+
FROM PIN 11
MODE SELECT AMPLIFIER
9
CONTROLS TYPE OF DISPLAY, BAR OR SINGLE LED
V− 2
BUFFER
SIG IN 5
20k

Figure 4-12. LM3914 block diagram
Courtesy of National Semiconductor Corporation

Block Diagram (Showing Simplest Application)

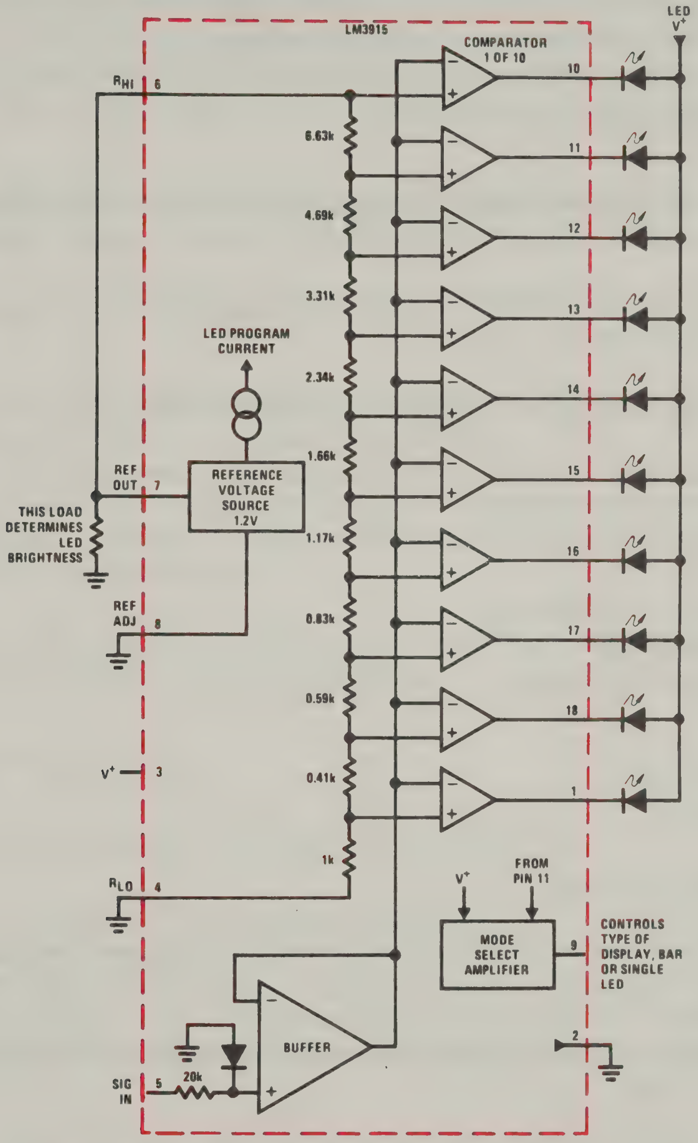

LM3915
COMPARATOR
1 OF 10
LED
V$^+$
R_{HI}
6
6.63k
4.69k
3.31k
2.34k
1.66k
1.17k
0.83k
0.59k
0.41k
1k
10
11
12
13
14
15
16
17
18
1
LED PROGRAM
CURRENT
REFERENCE
VOLTAGE
SOURCE
1.2V
REF
OUT
7
THIS LOAD
DETERMINES
LED
BRIGHTNESS
REF
ADJ
8
V$^+$
3
R_{LO}
4
V$^+$
FROM
PIN 11
MODE
SELECT
AMPLIFIER
9
CONTROLS
TYPE OF
DISPLAY, BAR
OR SINGLE
LED
BUFFER
2
SIG
IN
5
20k

Figure 4-13. LM3915 block diagram
Courtesy of National Semiconductor Corporation

As shown in **Figure 4-13**, the operation of the LM 3915 is nearly identical to the LM 3914. The difference between the two chips can be understood by comparing their internal voltage dividers. The 3914 uses ten equivalent resistors to produce linear output steps, while the 3915's voltage divider uses a logarithmic resistor relationship to produce output steps of 3 *dB* per step. The LM 3915 can be cascaded to provide displays with ranges from 60 to 90 *dB*. This ideally suits the 3915 to applications such as audio level and power meter displays.

Topic Review 4-6

1. A popular application of op amp comparators is the implementation of ______ ______ ______ .
2. These circuits consist of a calibrated ______ ______ , ______ ______ ______, and multiple colors of ______ .
3. The displays can be constructed to indicate either ______ or ______ scales.
4. In **Figure 4-11**, as the level in the gas tank decreases, V_{ref} ______ .

Answers:

1. multiple level displays
2. voltage divider
   op amp comparators
   LED's
3. linear
   logarithmic
4. decreases

4-7 Summary Points

1. Comparators are op amp circuits which compare two input voltages to each other, or compare an input voltage to an input reference voltage.
2. Comparators operate in the open-loop (no feedback) mode, using the full gain of the op amp.
3. The output of a comparator indicates the status of an input signal with relation to a reference voltage, and does not bear any indication on the type of input signal.
4. Simple comparators produce an output that is an indication of the relative polarities of the two input signals.

5. Zero crossing or ground detectors compare an input signal to ground. This is accomplished by grounding one of the op amp inputs. Whether the output is the same polarity or inverted depends upon which input the signal is applied to. In any level detector, the detector will be inverting if the signal is applied to the inverting input. The opposite holds true if the signal is applied to the non-inverting input.
6. Any voltage level, for either a positive or negative voltage level detector, can be implemented by establishing a reference voltage with a resistive voltage divider.
7. A simple comparator can be used to detect phase difference between two input signals.
8. Window detectors can be constructed to monitor a signal and indicate when the signal is either within or outside of preset voltage limits.
9. Multiple level indicators are constructed by using op amp comparators. These compare an input signal voltage to voltage references, which are established by a multiple-step resistive voltage divider.
10. IC manufacturers produce a line of both linear (equal step) and decibel (logarithmic step) ten-level bar graph/dot display drivers

4-8 Chapter Progress Evaluation

1. In **Figure 4-1**, if R_1 equals 10 $k\Omega$, what is the value of R_2?
2. In **Figure 4-1**, V_{in_1} equals +4 VDC and V_{in_2} equals +3.5 VDC. To what approximate value will V_{out} be driven if $V-$ equals -15 VDC?
3. Assume the voltage level detector of **Figure 4-5** has been designed to detect +5.0 VDC, and that $V+$ equalks 12 VDC. What is the value of R_1, if R_2 equals 10 $k\Omega$ and R_{in} equals 10 $k\Omega$?
4. In **Figure 4-4a**, what is the value of V_{out} when the input signals are (**a**) in phase with each other and (**b**) 180° out of phase with each other?
5. Assume the voltage level detector of **Figure 4-5** has been designed to detect +5.0 VDC, and that $V+$ equals 12 VDC. What is the value of R_1, if R_2 equals 10 $k\Omega$ and R_{in} equals 10 $k\Omega$?

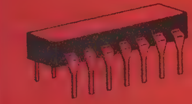
6. In **Figure 4-5**, find the value of V_{ref} if R_1 equals 12 $k\Omega$, R_2 equals 12 $k\Omega$, and $V+$ equals 10 VDC.

7. Using **Figure 4-8**, assume that V_{ul} equals +5.0 VDC and V_{ll} equals +4.0 VDC. Which of the following voltages would cause the LED to conduct?

8. In **Figure 4-11**, assume the tank is full. What is the value of V_{level} if R_{lim} equals 1 $k\Omega$ R equals 22 ohms, and the float resistance in the tank equals 178 ohms when the tank is empty?

9. When the tank is half full, what is the value of **(a)** V_{level} and **(b)** V_{ref}?

10. What is the level indication of the multiple-level indicator in **Figure 4-11**, if V_{level} equals 0.57 VDC and V_{ref} equals .62 VDC?



Chapter 5

Oscillators and Function Generators

Objectives

Upon completion of this chapter, you should be able to do the following:

- Distinguish between various op amp oscillators and list their applications
- Describe the operation of function generators and their uses, in particular, the 8038 IC function generator

5-1 Introduction

An oscillator is a circuit that converts a DC voltage into an AC or pulsating DC voltage. The frequency of oscillations may be anywhere from a few hertz to a million hertz, or even higher. A major requirement for an oscillator is that the output must be constant in both amplitude and frequency. In the study of oscillators, it will be seen that positive or regenerative feedback is needed to maintain oscillations. In fact, **positive feedback is the most important requisite for maintaining oscillator action.** Positive feedback is accomplished by taking a portion of the output signal and feeding it back into the input of the oscillator circuit in phase with the input signal.

When the product of the amplifier gain and the feedback factor equals 1, the oscillator will have infinite stage-gain. At first this may seem impractical, but it is actually a desirable condition and is required for oscillation. This requirement for oscillators is commonly referred to as "Barkhausen Criterion".

By connecting the inputs of an op amp to ground, through input resistors, we can cause the op amp to oscillate when it is initially turned on. This configuration introduces noise into the op amp, causing it to oscillate at all frequencies. These frequencies can then be fed to a frequency-selective network, similar to a very narrow (1 *Hz*) bandpass filter. The frequency-selective network is in the feedback path and allows only one frequency, the frequency of oscillation, to be fed back into the input. Because of the inherent 180° phase shift of the frequency selective network, the feedback signal is connected to the inverting input of the op amp. The feedback signal is now in phase with the input signal, and adds to it at the selected operating frequency. The frequency of oscillation regenerates itself; thus, we have "regenerative feedback." When signals out-of-phase are fed back into the input, the oscillations degenerate. Phase-signals such as these are known as "degenerative feedback."

It should be pointed out here, that in dealing with op amp oscillator networks, the noninverting input is not used alone in a feedback loop. Although it appears the natural choice for regenerative (in phase) feedback; remember, the frequency selective network has a natural 180° phase shift. To compensate for this phase shift, the inverting input is utilized.

Topic Review 5-1

1. ______ feedback is the most important requisite for maintaining oscillator action.

2. A major requirement for an oscillator is that the output must be constant in both ______ and freuqncy.

Answers:

1. Positive
2. amplitude

5-2 Active Wien-Bridge Oscillator

A practical Wien-bridge oscillator circuit is shown in **Figure 5-1.** This circuit uses *RC* networks in a bridge configuration to provide both regenerative and degenerative feedback (voltage). The network actually selects the frequency at which feedback occurs.

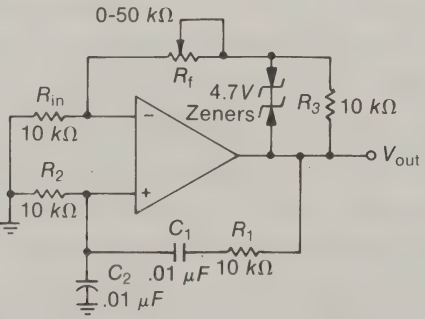


Figure 5-1. Active Wien-bridge oscillator

Regenerative feedback is applied to the noninverting input through the RC networks of R_1-C_1 and R_2-C_2. Degenerative feedback is fed to the inverting input of the op amp through R_f and R_3. Because the resistance values of R_f and R_3 will remain constant at all frequencies, the degenerative feedback is constant. However, the RC networks will vary the regenerative feedback with regard to frequency changes because of the capacitive reactance. By varying the setting of R_f, the desired operating frequency can be selected, because this frequency occurs when regenerative feedback is just larger than degenerative feedback. Once the value of R_f is set, if the oscillator frequency tries to increase, X_{C_2} will decrease and the regenerative voltage is shunted to ground, around R_2. Similarly, if the frequency tries to decrease, X_{C_1} will increase and the regenerative voltage is reduced again. Only at the oscillator frequency, will the RC networks allow enough regenerative feedback to sustain oscillation. By this operation, the oscillator is held on frequency.

The positive or regenerative feedback builds up over time. If left uncontrolled, this positive feedback would drive the output voltage to positive saturation. Back-to-back zener diodes are placed in the degenerative feedback circuit to regulate V_{out} to a useful amplitude. As the output voltage attempts to rise above the zener voltage, one of the diodes will break down and conduct. This shunts a portion of the negative or degenerative feedback resistance R_3, allowing more negative feedback to be applied to the op amp. This keeps the output from going to saturation and clipping the sine-wave.

The output frequency can be calculated by the formula:

$$f_{out} = \frac{1}{2\pi\sqrt{R_1\,R_2\,C_1\,C_2}} \tag{5-1}$$

When $R_1 = R_2$ and $C_1 = C_2$, f_{out} equals:

$$f_{out} = \frac{1}{2\pi\,R_1\,C_1} \tag{5-2}$$

The output frequency for the values given in **Figure 5-1** is approximately:

$$f_{out} = 1592\ Hz$$

Resistor R_f is made adjustable to control negative feedback when the circuit is first assembled. R_f is adjusted until the positive feedback overcomes the negative feedback and oscillation begins. After this initial set up, the circuit should be able to be powered down and restarted without further adjustment (bumping), to start oscillation. **This adjustment fulfills the Barkhausen Criterion, which states that the product of the amplifier gain and the feedback factor must equal one, for the oscillator to be self starting and self perpetuating.** The outstanding feature of the Wien-bridge oscillator is the low distortion sine-wave that it produces. To insure maximized performance and prevent loading, it is recommended that the output be followed by a buffer stage.

Topic Review 5-2

1. The Wien-bridge oscillator uses ______ networks that make up a bridge circuit to provide ______ and degenerative feedback.
2. The networks actually select the ______ at which feedback occurs.

Answers:

1. *RC*, regenerative
2. frequency

5-3 Active Crystal Oscillator

Crystals are natural oscillators because they produce mechanical oscillations which are extremely constant. These mechanical oscillations produce an electrical signal from the crystal. Also, a crystal will produce the mechanical oscillations (frequency) when subjected to a difference of potential across its faces. The natural frequency of a crystal is determined by its thickness. Generally, the thicker the crystal, the lower its natural frequency of oscillation; and therefore, the thinner the crystal, the higher its natural frequency. The highly stable frequency of the crystal provides very stable oscillator circuits. A more in-depth explaination of crystals can be found in the second book of this series, titled; Semiconductors, Circuits and Devices.

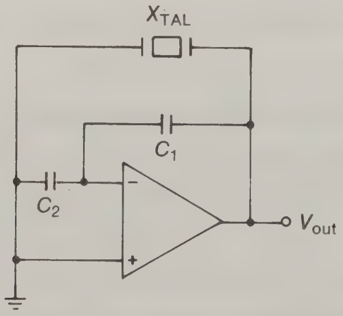


Figure 5-2. Active Pierce crystal oscillator

Figure 5-2 shows an active crystal oscillator configuration, known as the Pierce oscillator. The crystal is used as a frequency-sensitive variable impedance in parallel with a capacitive voltage divider. The crystal acts as an inductance in parallel with C_1 and C_2, forming a parallel-resonant tuned tank circuit. At the resonant frequency of the tank circuit, the feedback impedance is maximum and the crystal excitation voltage is determined by the ratio of C_1 to C_2. If the frequency attempts to increase or decrease (an undesirable frequency appears at the output), the impedance of the crystal decreases, decreasing feedback and shunting the undesired frequency to ground. The resonant frequency is shifted 180°, due to the inverting input and is shifted an additional 180° from the tuned tank circuit. Only the resonant frequency receives the complete 360° phase shift needed for oscillation.

The thickness of the crystal is the major factor in determining the resonant frequency of the device. The crystal may be used in either series of parallel-resonant configurations. The resonant frequency of the crystal will be slightly different for parallel configurations than for series configurations. The stability of crystal oscillators can be better than 0.0001%. Often, crystals are mounted in precision crystal ovens to provide stable operating temperatures and thereby increase oscillator stability.

Topic Review 5-3

1. A crystal produces extremely constant ______ ______ when subjected to a difference of potential across its faces.

2. In the Pierce oscillator, the crystal is used as a ______ sensitive, variable impedance.

3. In the Pierce oscillator; at the resonant frequency of the tank circuit, the feedback impedance is ______.

Answers:

1. mechanical oscillations
2. frequency
3. maximum

5-4 Square Wave Generators (Multivibrators)

A square wave generator is also referred to as a free-running or astable multivibrator. An op amp can be used to produce a multivibrator, as shown in **Figure 5-3.**

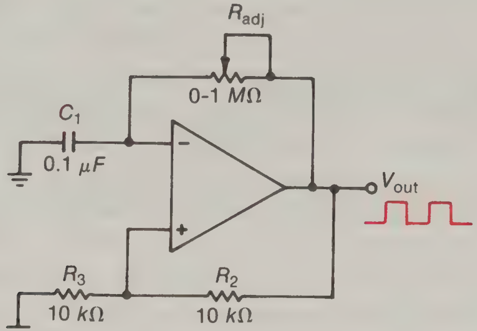


Figure 5-3. An astable multivibrator

In an astable device, the output will constantly change states, from high to low and back again without any input signal applied. Once again, the circuit is basically a comparator with noise induced into the input leads. When the circuit is energized, the op amp's output will swing either positive or negative toward saturation. This output will cause feedback to be applied to both inputs. A resistive voltage divider applies a reference voltage to the noninverting input while the capacitor, C_1, supplies the input voltage level to the inverting input. As feedback current begins to flow, capacitor C_1 charges until the voltage developed across it, slightly exceeds the reference voltage. At this point, the inverting input will cause the output polarity to reverse and the capacitor will charge in the opposite direction.

The output frequency of the circuit is dependent upon the *RC* time constant established by R_1 and C_1, and the value of the reference voltage. For the component values shown in the resistive voltage divider of **Figure 5-3,** the output frequency is calculated by:

$$f_{out} = \frac{1}{2.2\ R_1\ C_1} \tag{5-3}$$

R_1 is made variable to allow the output frequency to be varied.

5-5 Triangle Wave Generator

A circuit which produces triangle-waves can easily be constructed by combining the free-running multivibrator with an integrator, as shown in **Figure 5-4.** Recall that an integrator will produce a ramp output from a square-wave input.

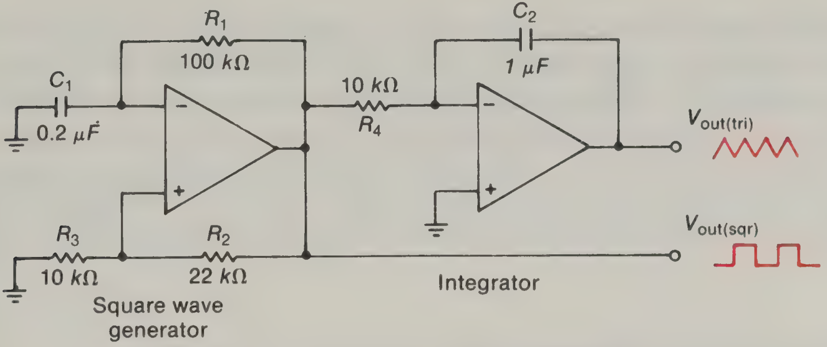

R_1
100 kΩ
C_1
0.2 μF
R_3
10 kΩ
R_2
22 kΩ
Square wave generator
10 kΩ
R_4
C_2
1 μF
Integrator
$V_{out(tri)}$
$V_{out(sqr)}$

Figure 5-4. A square/triangle-wave generator

The output frequency is calculated by:

$$f_{out} \cong \frac{1}{2.2\ R_1 C_1} \tag{5-4}$$

Another form of this generator is the hysteresis oscillator. The circuit contains a zero-level detector (square-wave generator) and an integrator, as shown in **Figure 5-5.**

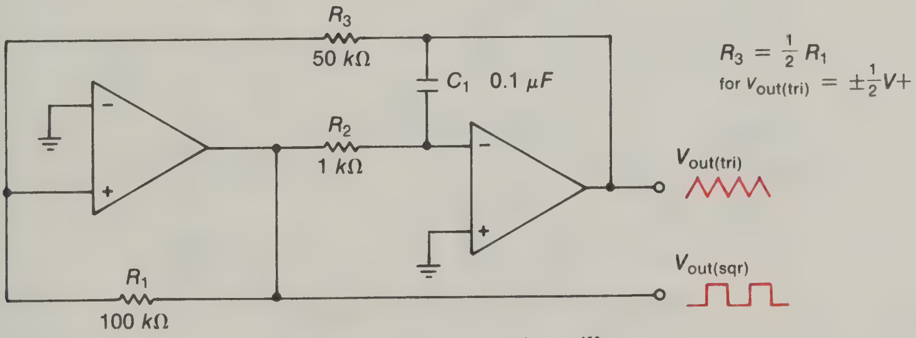

R_3
50 kΩ
C_1 0.1 μF
R_2
1 kΩ
R_1
100 kΩ
$V_{out(tri)}$
$V_{out(sqr)}$
$R_3 = \frac{1}{2} R_1$
for $V_{out(tri)} = \pm\frac{1}{2}V+$

Figure 5-5. Hysteresis oscillator

When the circuit is powered up, the output of op amp #1 will swing to plus or minus saturation. Current will flow through R_2 and C_1 causing the capacitor to charge. As C_1 charges, feedback is reduced causing $V_{out(tri)}$ to ramp downward. When $V_{out(tri)}$ has ramped down to approximately $\frac{1}{2}$ of $-V_{sat}$, the feedback through R_3 will cause the first op amp to swing negative. This in turn, causes $V_{out(tri)}$ to ramp upward until it reaches approximately $\frac{1}{2}$ of $+V_{sat}$, and the cycle will repeat. The frequency of the circuit can be calculated by:

$$f_{out} \cong \frac{1}{2R_2C_1} \tag{5-5}$$

Since the output polarities of the two op amps are always opposite, the level at which the integrator output will cause the zero-level detector to change states ($+\frac{1}{2}$ $V+$) can be adjusted by changing the ratio of the resistive voltage divider (R_3 to R_1).

A function generator is any signal generator that produces two or more different output waveforms. Therefore, the circuits shown in **Figures 5-4** and **5-5** qualify as function generators. Most often, two or more basic circuits are combined to form function generators. We will look at more examples in the next few topics.

5-6 Sine/Square-Wave Generator

A bandpass filter and a simple comparator are combined in **Figure 5-6** to form a sine/square-wave generator. The bandpass filter is used to produce the sine-wave which is applied to the inverting input of the comparator. The square-wave output is taken from the comparator output, and the sine-wave output is available from the output of the bandpass filter.

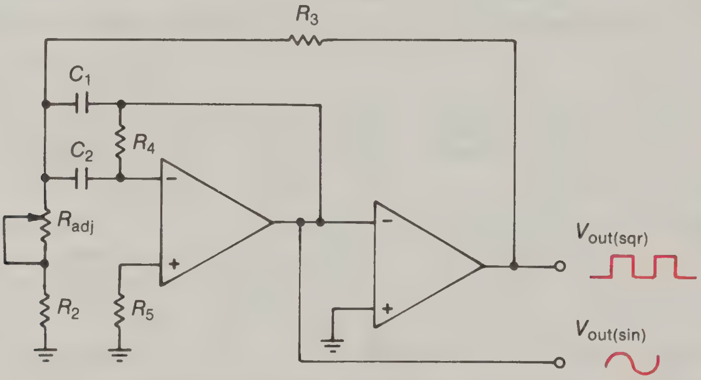


Figure 5-6. Sine/square-wave generator

A full discussion of how a bandpass filter produces a sine-wave from a square-wave would involve an extended calculus explanation. Stated simply, a square-wave consists of a basic sine-wave frequency, and an infinite number of harmonics of that basic frequency. We have seen how a narrow (1 *Hz*) bandpass filter can be used as a sine-wave oscillator. In this case, the filter strips all of the harmonics from the square-wave, leaving only the basic sine-wave frequency that the filter is tuned to pass.

The output frequency of both the square-wave and sine-wave is calculated by:

$$f_{out} = \frac{1}{2\pi\sqrt{R_p R_4 C_1 C_2}} \tag{5-6}$$

where parallel resistance =

$$R_p = \frac{R_3\,(R_{adj} + R_2)}{R_3 + R_{adj} + R_2} \qquad (5\text{-}7)$$

If: $R_{adj} = 0\text{-}50\ k\Omega$, let $R_{adj} = 25\ k\Omega$
$R_2 = 100\ \Omega$
$R_3 = R_4 = 1\ M\Omega$
$R_5 = 50\ k\Omega$
$C_1 = 0.01\ \mu F$
$C_2 = 0.01\ \mu F$
Then: $f_{out} = 100\ Hz$

R_{adj} is made adjustable to allow variation of the output frequency. Other frequencies may also be obtained by varying the values of C_1 and C_2.

5-7 Sine/Cosine-Wave Generator

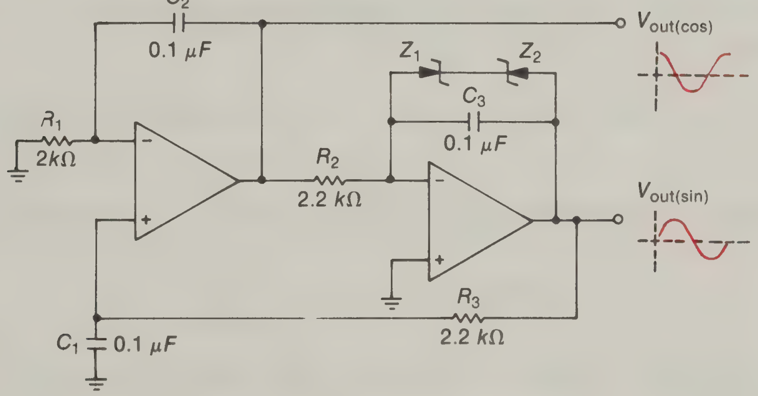


Figure 5-7. Quadrature oscillator

Another function generator is the sine/cosine-wave generator, shown in **Figure 5-7.** This generator produces two sine waves, 90° out of phase, and is also known as a quadrature oscillator. Noise is introduced into op amp #1 through its input leads. Both op amps are configured as integrators with long *RC* time constants. Long *RC* time constants are desirable to allow the capacitors to charge into the nonlinear portion of their charging curve. A shorter time constant, particularly for op amp #1, may result in a triangular output wave form.

Back to back zener diodes are placed in the feedback loop of the cosine integrator, op amp #2, to prevent the outputs from saturation, similar to the Wien-bridge oscillator. The output frequency can be calculated by:

$$f_{\text{out}} = \frac{1}{2\pi R_2 C_3} \tag{5-8}$$

where:

$$R_1 < R_2$$

$$R_2 = R_3$$

$$C_1 = C_2 = C_3$$

R_1 is made slightly less then R_2 to allow the oscillation process to begin when the circuit is powered up.

Topic Review 5-4 through 5-7

1. A square-wave generator is also known as an ______ multivibrator.

2. A triangle-wave generator may be constructed by combining an ______ multivibrator with an ______.

3. A ______ ______ filter and a simple ______ are combined to form a sine-wave generator.

4. The sine/cosine-wave generator is also known as a ______ oscillator.

Answers:

1. astable
2. astable, integrator
3. bandpass, comparator
4. quadrature

5-8 Three-Function Generator

In **Figure 5-8**, a bandpass filter is used to produce the sine-wave output and to provide the input frequency to the other two generators. The output of the sine-wave generator is applied to a buffer, op amp #2, which prevents circuit loading. From there it is applied to a simple comparator, op amp #3, which produces a square-wave output. Its output is then fed into an integrator, op amp #4, which produces a triangle-wave output.

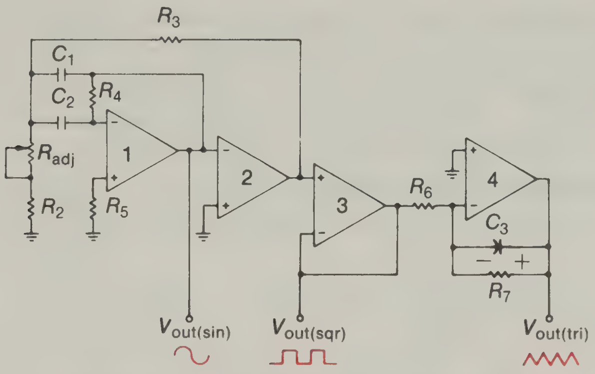


Figure 5-8. Three-function generator

The output frequencies can be calculated by:

$$f_{out} = \frac{1}{2\pi\sqrt{R_p\, R_4\, C_1\, C_2}} \tag{5-9}$$

$$\text{where: } R_p = \frac{R_3\,(R_{adj} + R_2)}{R_3 + R_{adj} + R_2} \tag{5-10}$$

A sample set of values:

$R_{adj} = 0\text{-}50\ k\Omega$
$R_2 = 100\ \Omega$
$C_1 = .1\ \mu F$
$C_2 = .1\ \mu F$
$R_3 = 1\ M\Omega$
$R_4 = 1\ M\Omega$

$R_5 = 50\ k$
$R_6 = 100\ k\Omega$
$R_7 = 470\ k\Omega$
$C_3 = .2\ \mu F$
$f_{out} \cong 7.5 - 1592 Hz$

This circuit can be constructed quite easily from a single IC by using a quad op amp IC such as the National Semiconductor LM324.

When designing op amp oscillators, special care should be taken when choosing an op amp for the application. Attention should be given to the unity-gain frequency of the op amp, slew rate, and whether the op amp has internal frequency compensation.

Topic Review 5-8

1. When designing op amp oscillators, attention should be given to the ______ ______ frequency of the op amp, ______ ______ and whether the op amp has internal ______ compensation.

Answers:

1. unity-gain, slew rate; frequency

5-9 The 8038 IC Function Generator

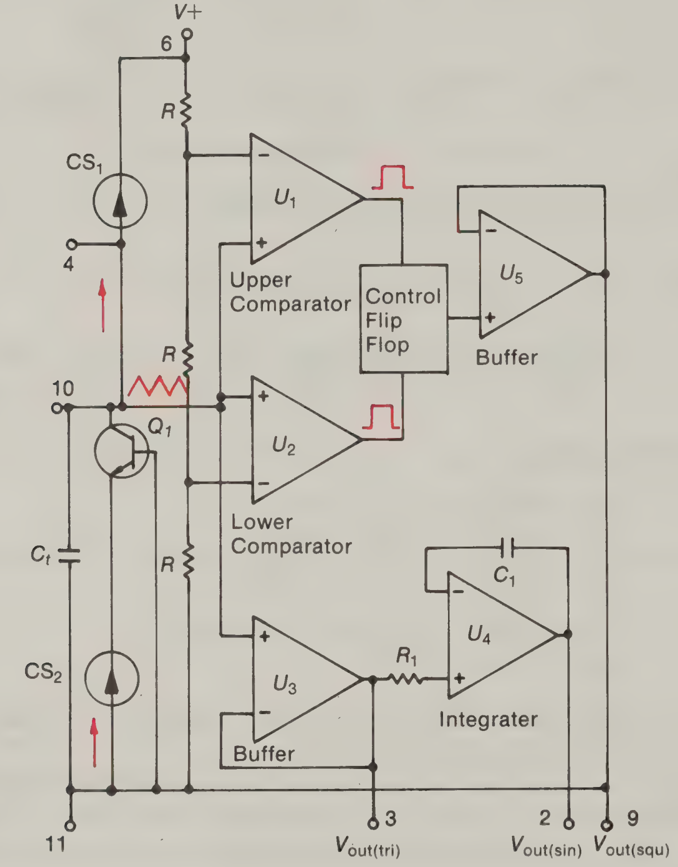

V+
6
R
CS$_1$
4
U$_1$
Upper
Comparator
Control
Flip
Flop
U$_5$
Buffer
R
10
Q$_1$
U$_2$
Lower
Comparator
C$_t$
R
C$_1$
U$_4$
CS$_2$
R$_1$
U$_3$
Integrater
Buffer
11
3
V$_{out(tri)}$
2
V$_{out(sin)}$
9
V$_{out(squ)}$

Figure 5-9. The 8038 function generator
Courtesy of Teledyne Corp.

The Intersil 8038 is an IC function generator, capable of producing sine, triangle, square, sawtooth and pulse waveforms, with a minimum of external components (See Figure 5-9). The 8038 features high accuracy, low distortion, low-frequency drift waveforms, over a wide frequency range. The 8038 can be operated with a wide range of single or dual supply voltages.

In **Figure 5-9**, an external timing capacitor, C_t, is charged and discharged at a linear rate between $\frac{1}{3}$ and $\frac{2}{3}$ of $V+$. The voltage across the timing capacitor is applied to an upper comparator, U_1, referenced at $\frac{2}{3}$ of $V+ -(V-)$, which is the absolute value of the power supply. The voltage across C_t is also applied to a lower comparator, U_2, referenced at $\frac{1}{3}$ of $V+ -(V-)$. The reference voltages are established by an equivalent three-resistor voltage divider. C_t is charged and discharged by the two constant current sources, CS_1 and CS_2, which causes the voltage across the capacitor to increase and decrease linearly.

The comparator outputs are used to trigger the control flip-flop. Each time one of the comparator outputs goes high, the output of the flip-flop changes state. The flip-flop's output is used to turn on and cut off transistor switch Q_1 and is buffered to provide the IC's square-wave output. Q_1 controls the charge and discharge of the timing capacitor.

When power is applied to the IC, the output of the flip-flop, U_6, is low, transistor Q_1 is cut off and the timing capacitor, C_t, begins charging through current source CS_1. The constant current, I, from CS_1, causes the voltage across C_t to increase at a linear rate. When the voltage exceeds $\frac{2}{3}$ $V+ -(V-)$, the upper threshold, V_{ut}, the output of the upper comparator goes high momentarily, causing the output of the flip-flop to go high. This turns on Q_1, causing C_t to discharge through CS_2 with a difference current of $I(I + I_{CS_2} = 2\,I_{CS_2})$. The C_t voltage will decrease linearly until it reaches $\frac{1}{3}$ $V+ -(V-)$, the lower threshold, V_{lt}. This causes the output of U_2, the lower comparator, to go high momentarily. This triggers the flip-flop, resetting its output to the low state, and begins a new cycle.

The voltage developed across C_t is fed through a buffer and used as the triangle-wave output. The output of the control flip-flop, which changes states from high to low and back, is also buffered and used as the square-wave output. The triangle-wave output is applied to an integrator circuit, which produces the sine-wave output.

As shown in **Figure 5-10**, the ratio of the constant current sources can be reprogrammed with the addition of external timing resistors, between pins 4 and 5 and $V+$. Resistor R_A, connected to pin 4, controls the rising portion of the triangle-wave R_B, connected to pin 5, controls the declining portion of the wave. Since the triangle-wave controls the timing of the other waveforms, the relationship of R_A and R_B will determine the symmetry and duty factor of the sine and square waves. When R_A equals R_B, symmetrical sine, triangle, and square waves, with a 50% duty factor, are produced.

The rising portion of the sine and triangle waves, and the "up" time of the square wave, can be calculated by the formula:

$$t_1 = 1.67\,R_A C_t \tag{5-11}$$

The falling portion of the sine and triangle waves and the "low" time of the square-wave can be found from the formula:

$$t_2 = 1.67 \left(\frac{R_A R_B C_t}{2R_A - R_B}\right) \tag{5-12}$$

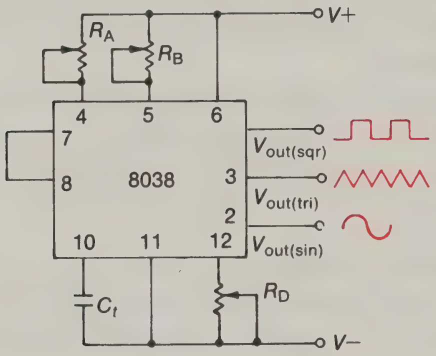


Figure 5-10. Typical 8038 configuration

The configuration shown in **Figure 5-10** allows duty-factor adjustment from less than 1% to greater than 99%. Resistor R_D is used to minimize sine-wave distortion and is typically around 82 *k* ohms. The frequency of the output can be determined by applying the t_1 and t_2 to the frequency formula:

$$f_{out} = \frac{1}{t_1 + t_2} \tag{5-13}$$

$$f_{out} = \frac{1}{1.67 R_A C_t \left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

$$f_{out} = \frac{1}{1.67 R_A C_t \left(\frac{1 + R_B}{2R_A} - \frac{R_B}{R_B}\right)}$$

$$f_{out} = \frac{1}{1.67 R_A C_t \left(\frac{R_B}{2R_A}\right)}$$

$$f_{out} = \frac{1}{1.67 C_t \quad \left(\frac{R_B}{R_A}\right)}$$

$$f_{out} = \frac{R_A}{1.67 C_t R_B}$$

When choosing timing components R_A, R_B and C_t, it should be noted that charging currents between $10\mu A$ and $1\ mA$ provide maximum performance. C_t should be chosen as large as possible, while still allowing R_A and R_B to limit current to within the desirable range.

$$R_A = \frac{V+}{5\ I\ (\text{limit})}$$

$$R_B = \frac{V+}{5\ I\ (\text{limit})}$$ Pins 7 & 8 must be shorted together.

If no variation of the symmetrical waveforms is desired, the 8038 may be configured as shown in **Figure 5-11.**

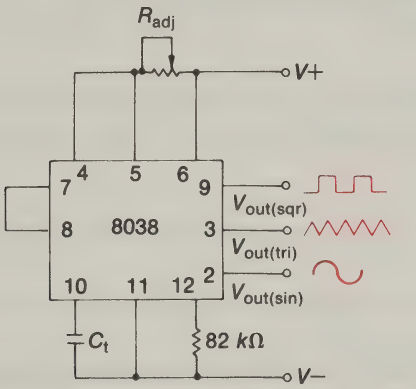


Figure 5-11. Symmetrical waveform 8038 configuration

The output frequency of this configuration is simply:

$$f_{out} = \frac{0.15}{R_{adj}C_t} \tag{5-14}$$

Topic Review 5-9

1. The Intersil 8038 is an IC function generator, capable of producing ______, ______, ______, ______, and ______ waveforms, with a minimum of external components.

2. An external timing capacitor (C_t) is charged and discharged by two ______ ______ sources. This causes the voltage across the capacitor to increase and decrease ______.

3. The voltage developed across C_t is fed through a buffer and used as the ______-wave output.
4. The output of the control flip-flop, is also buffered and used as the ______-wave output.
5. The triangle-wave output is applied to an integrator circuit, which produces the ______-wave output.

Answers:

1. sine, triangle, square, sawtooth and pulse
2. constant current, linearly
3. triangle
4. square
5. sine

5-10 Summary Points

1. Oscillators must have amplification and regenerative (in-phase) feedback.
2. The frequency of oscillation is determined by a frequency-selective network.
3. The Barkhausen Criterion says that the product of the amplifier gain and the fractional feedback factor must equal one for the oscillator to be self starting and self sustaining.
4. Inductors are not desirable in IC circuits. This tends to eliminate many LC oscillator circuits that are used with discrete circuitry. In some situations, standard LC oscillator configurations may be used in conjunction with the operational amplifier.
5. Sine-wave oscillators act like a 1 *Hz* bandpass filter.
6. The Wien-bridge oscillator uses both regenerative and degenerative feedback to produce a very low-distortion sine-wave output.
7. Crystal oscillators produce very stable output frequency sine-waves, due to the stability of the crystal's natural frequency of vibration.

8. A bandpass filter can be used to produce a sine-wave output from a square-wave input.

9. Back-to-back or face-to-face zener diodes may be used to limit oscillator output and prevent clipping of the sine-wave, due to output saturation.

10. Function generators are circuits that produce two or more output waveforms.

11. Square-waves are produced with op amp comparators (zero-level detectors).

12. Op amp integrators are used to produce sine and triangle waveforms.

13. Two integrators with regenerative feedback are used to produce two sine-waves, 90° out of phase (quadrature).

14. A three-function generator can be constructed from a bandpass filter, a zero-level detector, and an integrator, to produce sine, square, and triangle-waves simultaneously.

15. The ICL 8038 function generator provides three-function generation from a single chip.

5-11 Chapter Progress Evaluation

1. If in **Figure 5-1,** R_1, C_1, R_2 and C_2 equal 10 $k\Omega$, 0.01 μF, 20 $k\Omega$, and 0.01 μF, respectively, f_{out} would then equal:

2. What is the operating frequency of the astable multivibrator or square-wave generator of **Figure 5-3,** if R_1 is adjusted to 25 $k\Omega$ and C_1 equals 0.01 μF?

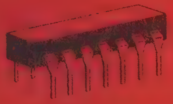
3. In the sine/square-wave generator of **Figure 5-6,** find f_{out} if R_1 and R_2 equals 10$k\Omega$, R_3 and R_4 equals 100 $k\Omega$, and C_1 and C_2 equals 0.01 μF.

4. If a crystal is replaced with one which is thicker, what effect will this have on the output frequency of the oscillator in which it is used?

5. What is a quadrature oscillator?

6. Name two types of circuits used to produce sine-waves.

Chapter 6



Active Filters

Objectives

Upon completion of this chapter, you should be able to do the following:

- Explain filter fundamentals
- Define first, second, and multi-order filter operation
- List special active filters and their applications

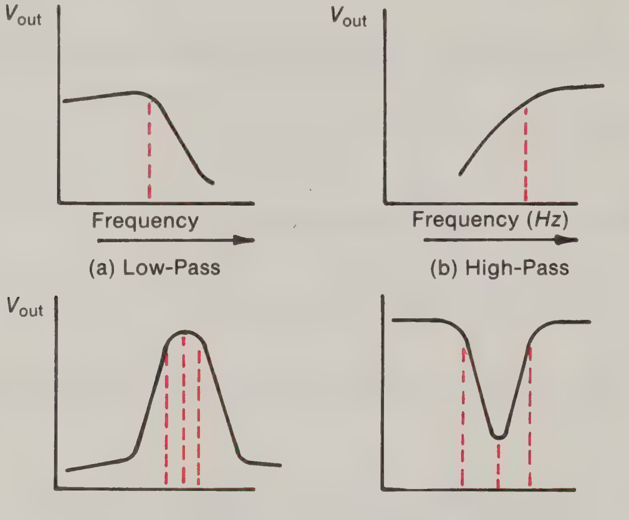
6-1 Introduction

A *filter* is a device that is designed to separate a desired quantity from an undesired quantity. An oil filter separates dirt and sludge from oil, and an air filter separates dust and vapors from air. These filters accomplish their design intentions by allowing the desired quantities to pass through the filter virtually unaffected, while blocking out the undesirable quantities. **An electronic filter is a frequency selective device that is designed to allow a desired group of frequencies to pass through the filter, while blocking all undesired frequencies.** Unfortunately, just as oil and air filters can't completely block out all undesirable elements, electronic filters do not completely block out all undesired frequencies.

Electronic filters fall into two broad catagories: passive and active. Passive filters are constructed from resistors, capacitors and inductors only, and are referred to as *RCL* filters. Active filters use capacitors and resistors with active elements, such as transistors and op amps. Inductors are not used in active filters, because they tend to be bulky, costly, and difficult to incorporate into integrated circuits. They also tend to have large values of resistance (low quality or *Q*).

Active filters have greater sensitivity and the ability to produce output signals larger than their input signals, but there are some drawbacks and limitations associated with active filters. Active filters require a power supply, generate noise, and are sensitive to component aging and thermal drift. Their applications are also limited to frequencies below 100 *kHz* and generally below 1 *kHz*. Op amps are used if the filter application needs high slew rates. These op amps may need to be the non-internally frequency compensated type.

Filters are further divided into four catagories: low-pass, high-pass, bandpass, and band-reject (notch), which produce voltage-to-frequency response curves like those shown in **Figure 6-1.**



(a) Low-Pass (b) High-Pass

(c) Band pass (d) Band-Reject (Notch)

Figure 6-1. Filter response curves

Topic Review 6-1

1. An electronic filter is a ______ selective device that is designed to allow a desired group of frequencies to pass, while blocking all undesired frequencies.

2. Electronic filters fall into two broad categories: ______ and ______.

3. Active filters have the advantages of greater ______ and the ability to produce output signals larger than their input signals.

Answers:

1. frequency
2. passive, active
3. sensitivity

6-2 Low-Pass Filters

From the characteristic response curve in **Figure 6-1a,** it can be seen that a low-pass filter provides a nearly constant output voltage, as frequency increases from DC up to a desired cutoff frequency (f_c) and attenuates frequencies above f_c. Ideally, a low-pass filter would pass all frequencies up to f_c and completely reject all frequencies above f_c.

The group of frequencies that a filter allows to pass through it unaffected is termed the filter's *passband*. The frequencies that the filter attenuates are called the *stopband*.

A simple, passive low-pass filter is shown in **Figure 6-2.**

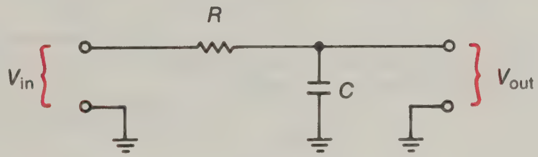


Figure 6-2. Simple low-pass filter

This filter utilizes the capacitor's inherent opposition to low frequencies,to develop high proportions of the signal voltage at low frequencies. The output is taken parallel to the capacitor; so, for low frequencies, a large proportion of the input signal will appear at the output. R is used simply to allow voltage distribution. The voltage dropped across the resistor is inversely proportional to the voltage developed across the capacitor. Ideally,this filter passes all frequencies up to f_c and wiil not pass any frequency above that point. But practically, the filter attenuates the signal more as the frequency increases above f_c.

Because the filter depends on the reactance (opposition to current) of the capacitor and the resistance (opposition to current) of the resistor to cause voltage division, f_c occurs where the opposition, due to the capacitor, equals the resistance ($X_C = R$). From the formula for capacitive reactance:

$$X_C = \frac{1}{2\pi f_c C} \tag{6-1}$$

$$R = \frac{1}{2\pi f_c C} \tag{6-2}$$

$$\text{therefore: } f_c = \frac{1}{2\pi RC} \tag{6-3}$$

At this point, the voltage dropped across the resistor becomes equal to the voltage across the capacitor. f_c is also known as the 0.707 frequency, the half-power frequency, the corner frequency, and the $3dB$ down frequency.

At frequencies above f_c, the capacitor develops less voltage, causing increasing amounts of the signal to be dropped across the resistor. **This gradual increase in attenuation of the signal, as frequency increases, is called *rolloff*.**

Figure 6-3 shows a simple, active, first-order, low-pass filter. In this configuration, the filtering is still being done be the RC network; the op amp is being used as a buffer for the filter which prevents loading of the filter output.

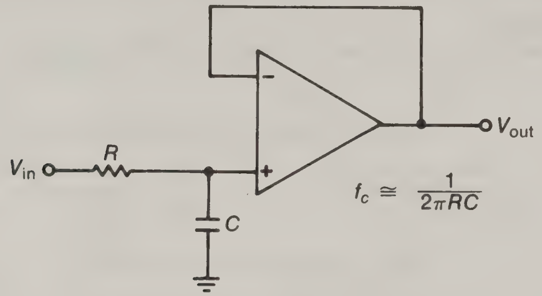


Figure 6-3. A simple active low-pass filter

The order of a filter is an indication of how steeply the output rolls off above f_c. This filter will have a rolloff of approximately $-20\ dB/$decade. This indicates that as the frequency increases by a factor of ten, above f_c, the output voltage decreases by 20 decibels. The greater the order of the filter, the faster the output rolloff. Remember that, ideally, we would like the output to drop to zero at one hertz above f_c, so, it is desirable to have the greatest decrease per decade as possible.

An active second-order low-pass filter can be designed by using the op amp's feedback characteristics to increase filtering. **Figure 6-4** shows a Butterworth-type, second-order, low-pass filter, which has a rolloff of approximately $-40dB/$decade. In this configuration, the op amp is actively participating in the filtering process.

Resistor R_2 and capacitor C_2 form the passive low-pass filter input to the noninverting input terminal. Resistor R_3 is chosen to form a noninverting voltage follower with R_1 and R_2 ($R_3 = R_1 + R_2$). It also diminishes any DC offset for the circuit.

R_1 and C_1 are added to the circuit to increase the filtering action. For frequencies above f_c, X_{C_2} decreases, causing the noninverting input to approach ground potential. As the noninverting input approaches ground, the inverting input will approach virtual ground, due to the zero voltage-differential characteristic of the op amp. More input current will flow through C_1 because V_{C_1} is also decreasing and the inverting input is approaching virtual ground. This input current is drawn away from the passive filter, causing further attenuation of the signal and increased rate of rolloff.

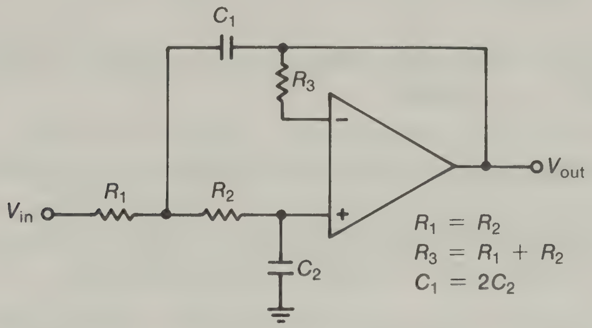

C_1
R_3
V_{out}
R_1
R_2
V_{in}
C_2
$R_1 = R_2$
$R_3 = R_1 + R_2$
$C_1 = 2C_2$

Figure 6-4. Butterworth second-order low-pass filter

f_c is approximated by the formula:

$$f_c = \frac{1}{2\pi\sqrt{R_1R_1C_1C_2}} \tag{6-4}$$

This formula is only valid where $R_1 = R_2$ and C_1 is greater than C_2. $C_1 = 2C_2$ is a suggested value.

By cascading (placing the output of one filter into the input of another) a second-order filter with a first-order filter, as shown in **Figure 6-5**, a third-order filter is achieved, with a rolloff of approximately $-60\ dB/$decade.

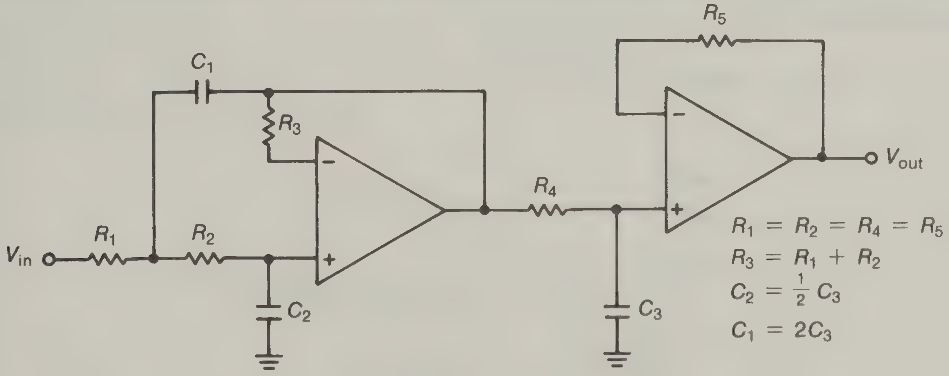

R_5
C_1
R_3
V_{out}
R_4
R_1
R_2
V_{in}
C_2
C_3
$R_1 = R_2 = R_4 = R_5$
$R_3 = R_1 + R_2$
$C_2 = \frac{1}{2} C_3$
$C_1 = 2C_3$

Figure 6-5. Third-order low-pass filter

Notice that C_1, C_2 and C_3 have different relationships than when either filter was used alone. This is necessary to produce a flat-line frequency response in the passband.

Topic Review 6-2

1. The group of frequencies that a filter allows to pass through it unaffected is termed the filter's ______ band.

2. The frequencies the filter attenuates are called its ______ band.

3. The f_c or cutoff frequency of the filter, is also known as the ______ frequency, the ______-______ frequency, and the 3 *dB* down frequency.

4. The gradual increase in attenuation of the signal as frequency increases is called ______.

Answers:

1. pass
2. stop
3. 0.707, half-power
4. rolloff

6-3 High-Pass Filters

High-pass filters perform exactly opposite to low-pass filters; ideally, they pass all frequencies above f_c and attenuate frequencies below f_c as shown by the response curve in **Figure 6-6.**

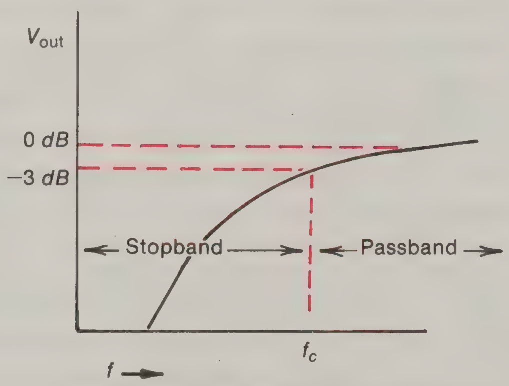


Figure 6-6. High-pass filter response curve

The stopband is located at the lower end of the frequency spectrum and the passband occupies the upper end. Rolloff occurs as frequency decreases below f_c.

A simple, passive, high-pass filter is shown in **Figure 6-7.**

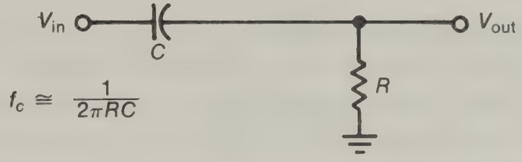


Figure 6-7. A passive $-20\ dB$/decade high-pass filter

This curcuit uses the same components as the low-pass filter, except that the output of the filter is now taken across the resistor instead of the capacitor. Remember from the low-pass filter, that the proportion of the signal voltage dropped across the resistor, was inverse to the voltage developed across the capacitor.

An active, $-20dB$/decade high-pass filter can be constructed by reversing the resistor and capacitor positions of the low-pass filter, as shown in **Figure 6-8.**

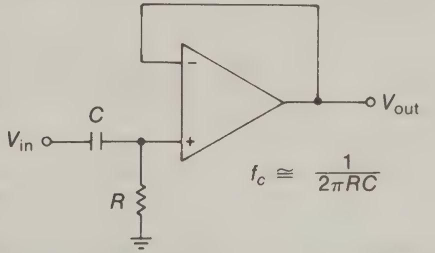


Figure 6-8. A simple active high-pass filter

From DC up to f_c, the input capacitor's reactance will be high, causing the capacitor to drop most of the signal voltage. Therefore, only a small portion of the signal will be applied to the buffer. As the input frequency increases above f_c, the capacitive reactance (X_C) decreases, allowing more of the signal voltage to be dropped across the resistor, which supplies the input voltage to the buffer.

Once again, the rolloff can be increased by using the op amp in the actual filtering process, as in **Figure 6-9.**

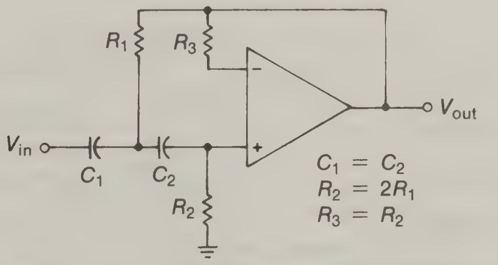


Figure 6-9. Second-order high-pass filter

Capacitor C_1 and resistor R_1 form one filter branch, and C_2 and R_2 form the op amp input filter. In this configuration, C_1 should equal C_2, and R_2 should be twice as large as R_1. R_3 is added for DC offset and should equal R_2.

f_c can be approximated by the formula:

$$f_c = \frac{1}{2\pi C\sqrt{R_1 R_2}} \tag{6-5}$$

for the relationships stated above.

As was the case with low-pass filters, a second-order filter can be cascaded with a first-order filter to produce a third-order high-pass filter, with −60 dB/decade rolloff. This is shown in **Figure 6-10.**

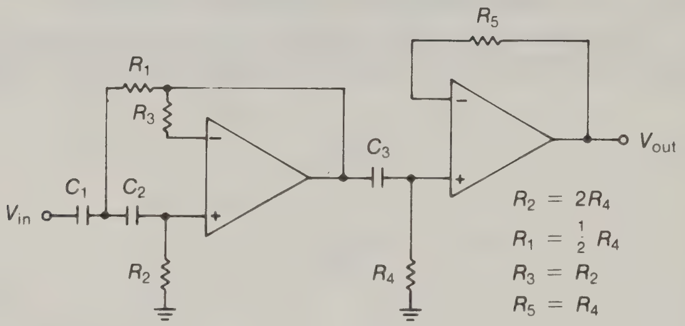


Figure 6-10. Third-order high-pass filter

For convenience, let's use the following relationships:

let $C_1 = C_2 = C_3$
calculate R_4 for f_c — choose some convenient value

let $R_1 = 2R_4$
$R_1 = \frac{1}{2} R_4$
$R_3 = R_2$
$R_5 = R_4$

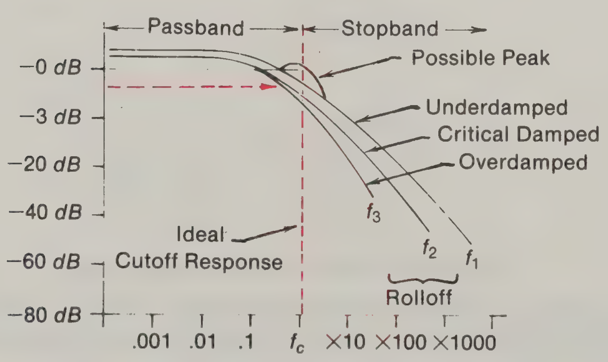


Figure 6-11. Typical low-pass response curves

The component relationships given for the filters discussed so far provide a Butterworth or flat-line frequency response. The response curves of these filters remain extremely flat (level) throughout their passbands. Other component relationships will render response curves less flat across the passband. See **Figure 6-11**

This figure shows three possible low-pass responses with identical cutoff frequencies. Curve f_1 shows a passband where the gain decreases as the frequency increases. Curve f_2 shows a response rising just before cut-off and curve f_3 depicts a Butterworth response remaining constant throughout the passband. Filter *damping* is a description of the filter's passband response. The flatter the response curve, the higher the damping.

Rolloff is a description of how much the filter attenuates the input signal as frequency exceeds f_c. Rolloff is expressed in terms of *dB/*decade and is calculated by:

$$\text{rolloff} = -20 \log \frac{V_{\text{out}}}{V_{\text{in}}} \tag{6-6}$$

A decade is a frequency increase of times ten above f_c. This is the frequency at which V_{out} is measured to determine rolloff.

The procedure for designing any of these filters for a specific application is fairly straightforward. First, choose the basic circuit configuration which fits the application. Next, choose a convenient value of capacitor or capicitors. From the formulas, calculate the values of resistance necessary to complete the filter.

As an example, let's design a third-order high-pass filter with a frequency cutoff of 1 *kHz*. The basic configuration of a third-order high-pass filter, is a second-order high-pass filter cascaded with a first-order high-pass filter. $C_1 = C_2 = C_3$. Let's choose a $0.01\mu F$ capacitor. Also, we will want the filter to have a rolloff response of -40 *dB/*decade. Therefore:

$$f_c = \frac{1}{2\pi C\sqrt{R_1 R_2}} \tag{6-7}$$

$$\text{and, } R_2 = 2R_1$$

$$\text{therefore: } f_c = \frac{1}{2\pi C\sqrt{R_1(2R_1)}} \tag{6-8}$$

$$f_c = \frac{1}{2\pi C\sqrt{2R_1{}^2}} \tag{6-9}$$

$$f_c = \frac{1}{2\pi C\,(1.414)\,R_1}$$

$$\text{so:} \quad 1\,kHz = \frac{1}{2\pi\,(1.414)\,(0.01 \times 10^{-6})}$$

$$\text{so:} \quad R_1 = \frac{1}{2\pi\,(1.414)\,(0.01 \times 10^{-6})\,(1 \times 10^{3})}$$

$$R_1 = 11.3\,k\Omega$$

because: $R_1 = \frac{1}{2}R_4$ then $R_4 = 22.6\,k\Omega$
and: $R_4 = R_5$ therefore $R_5 = 22.6\,k\Omega$
and: $R_2 = 2R_4$ therefore $R_2 = 45.2\,k\Omega$
and: $R_3 = R_2$ therefore $R_3 = 45.2\,k\Omega$

Higher order filters may be constructed in the same manner as the third-order filters. A fourth-order filter would be constructed by cascading two second-order filters. A fifth-order filter would require cascading two second-order filters, a first-order filter, and so on.

Another method of designing second-order high and low-pass filters is the equal component design configuraton. With this configuration the frequencies determining resistors and capacitors are made equal, and the passband gain is determined by a noninverting amplifier configuration, as shown in **Figure 6-12**. In order to achieve a Butterworth response, the gain of the filter should be held to unity in the passband.

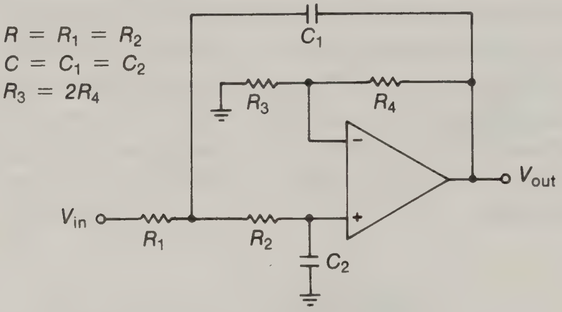


Figure 6-12. An equal component low-pass filter

The equal-component method simplifies circuit design, since R_1 equals R_2 and C_1 equals C_2. The cutoff frequency can now be calculated by:

$$f_c = \frac{1}{2\pi RC} \tag{6-10}$$

The gain of the filter is designed by setting the gain formula of a noninverting amplifier approximately equal to 1.5.

$$A_v = \frac{R_4}{R_3} + 1 \tag{6-11}$$

$$1.5 = \frac{R_4}{R_3} + 1$$

$$\frac{R_4}{R_3} = .5$$

$$R_4 = .5\,R_3$$

A high-pass equal-component filter is designed in the same manner as the low-pass filter. Resistive and capacitive frequency-determining components are exchanged and the passband gain is held at 1.5, as shown in **Figure 6-13.**

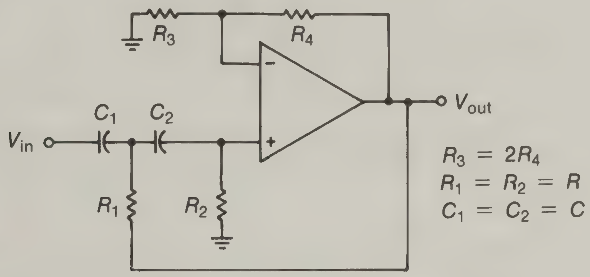


Figure 6-13. An equal component high-pass filter

The cutoff frequency is determined by:

$$f_c = \frac{1}{2\pi\,RC} \tag{6-12}$$

and passband gain by:

$$A_v = \frac{R_4}{R_3} + 1 \tag{6-13}$$

The design procedure is the same for both the high and low-pass equal component filters, so let's design a low-pass filter to have a cutoff frequency of 1 *kHz*.

First choose a capacitor:

let's choose $C = C_1 = C_2 = 0.01\mu F$

Next, calculate the resistor values:

$$f_c = \frac{1}{2\pi\,RC} \tag{6-14}$$

$$R = \frac{1}{2\pi f_c C} \tag{6-15}$$

$$R = \frac{1}{2\pi\,(1k')\,(0.01\mu F)}$$

$$R = 15.900\ \Omega = R_1 = R_2$$

Resistors for the feedback loop should be chosen between 10 $k\Omega$ and 50 $k\Omega$. In order to fulfill the design requirements, let R_3 equal 47 $k\Omega$. Therefore, R_4 should be equal to 23.5 $k\Omega$; the nearest standard resistor value would be 22 $k\Omega$. This completes the design which is shown in **Figure 6-14.**

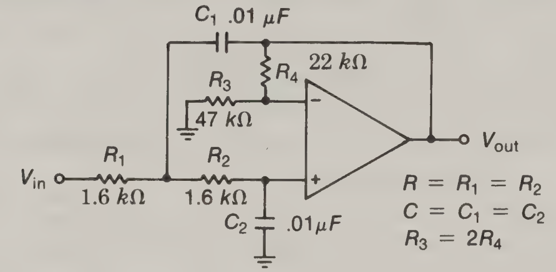


Figure 6-14. Circuit design of equal component filter

Topic Review 6-3

1. A ______ is a frequency increase of ten times above f_c. This is the frequency at which V_{out} is measured to determine rolloff.

2. A fourth-order filter can be constructed by cascading two ______-order filters.

Answers:

1. decade
2. second

6-4 Bandpass Filters

So far, we have used filters to separate the frequency spectrum into highs and lows. In many instances, it is desirable to pass a band of frequencies in the spectrum, while rejecting the very high and very low frequencies of the spectrum. An example is the midrange of a three-way crossover speaker network.

This is accomplished with a bandpass filter. Passive bandpass filters use inductors and capacitors to cause the voltage to rise in the middle of the frequency spectrum. The center of this voltage rise is known as resonance, where $X_C = X_L$.

In active circuits, inductors are not used, so other means must be employed to cause this voltage rise and therefore produce a passband. Recall that the passband contained the frequencies that produced an output voltage above 70.7% of the maximum voltage.

With a bandpass filter the passband lies between the point where the characteristic curve rises above 70.7% of max (f_{low}) and where the curve dips below 70.7% (f_{high}). This is shown in **Figure 6-15.**

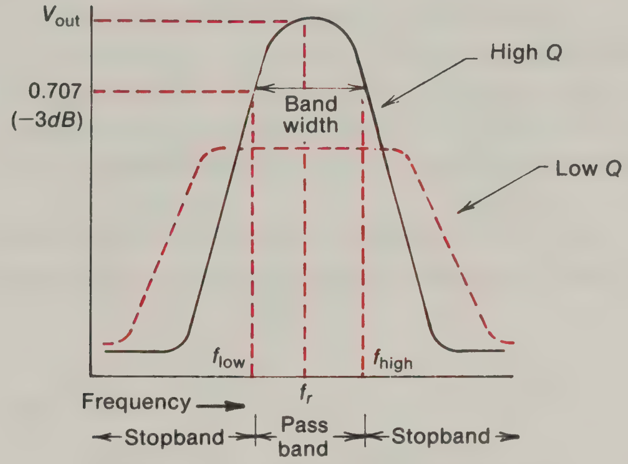


Figure 6-15. Bandpass filter response curve

The distance between f_{low} and f_{high} is the bandwidth (measured in *Hz*) of the filter. In the center of the bandwidth is the resonant frequency (f_r) or center frequency.

Bandwidth is calculated by:

$$\text{Bandwidth} = f_{\text{high}} - f_{\text{low}} \tag{6-16}$$

If the bandwidth is less than 10% of f_r, the filter is a narrow band-pass filter and if it is greater than 10% of f_r, the filter is classified as a wide bandpass filter.

An important consideration when using a bandpass filter is its selectivity. **Selectivity is the ability of a filter to pass a selected frequency and reject all other frequencies, and is expressed as the quality of the filter (Q).** Quality can be determined by the formula:

$$Q = \frac{f_r}{\text{BW}} \tag{6-17}$$

Quality is not an indication of how useful or precise the filter is, but is an expression of bandwidth and output voltage.

High Q filters tend to have narrow bandwidths and large V_{outs}, while low Q filters have wider bandwidths and tend to produce less V_{out}.

A bandpass filter can be constructed by combining an active low-pass filter and an active high-pass filter. This is shown in **Figure 6-16.**

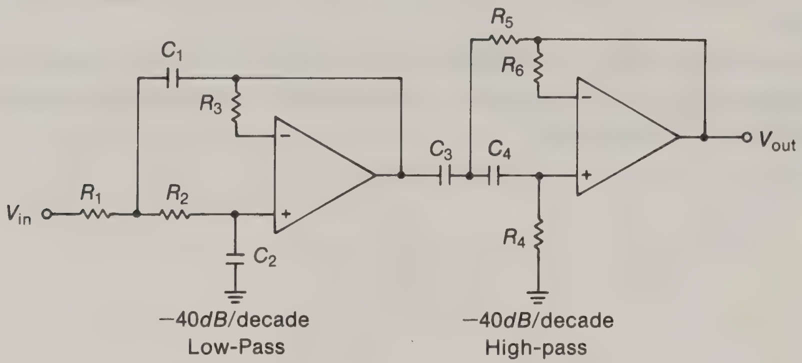


Figure 6-16. Two op amp bandpass filter

The f_c for each circuit should be calculated to produce the response curves shown in **Figure 6-17.**

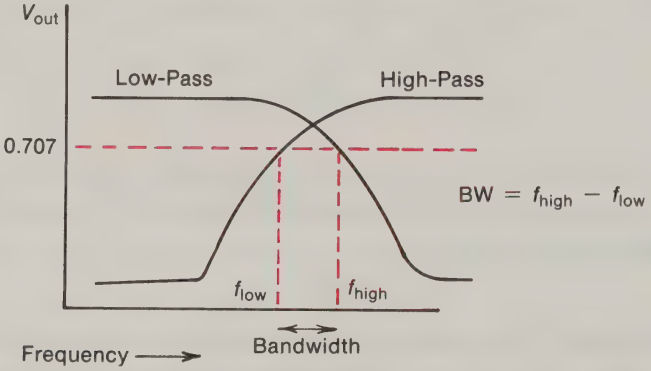


Figure 6-17. Active low-pass and high-pass, bandpass filter response curves

By causing the response curves to overlap, the high-pass filter will attenuate frequencies below f_{low} and the low-pass filter will attenuate frequencies above f_{high}. The f_{low} equals f_c of the high-pass, and f_{high} equals f_c for the low-pass. The f_r will be halfway between f_{low} and f_{high}.

The bandwidth is easily manipulated in this configuration by changing values of R and C within each of the filters, to adjust f_{low} and f_{high} as desired. The formulas for high and low-pass filters (previously covered) should be used. A buffer can be included between the stages to minimize signal loss between stages.

A single-stage, bandpass filter can also be constructed, as shown in **Figure 6-18.**

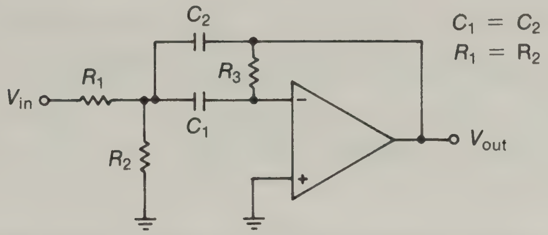


Figure 6-18. Single-stage op amp bandpass filter

In this configuration, R_1 and C_2 provide low-pass filtering by allowing more degenerative feedback as frequency increases. R_2 and C_1 provide high-pass filtering (C_1 attenuates low frequency). R_3 provides gain for the circuit and establishes Q and f_r. When R_3 is small, f_r will be high and Q will be low. When R_3 is large, f_r is low and Q is high.

f_r can be calculated by:

$$f_r = \frac{1}{2\pi\sqrt{R_p R_3 C_1 C_2}} \tag{6-18}$$

$$\text{where } R_p = \frac{R_1 R_2}{R_1 + R_2} = \tfrac{1}{2}R_1 \text{ if } R_1 = R_2 \tag{6-19}$$

Q can be found by:

$$Q = .5\sqrt{\frac{R_3}{R_p}} \qquad \text{when } C_1 = C_2$$

Remember, Q is an expression of bandwidth. In audio applications a highly selective filter is desirable, while in television, where a much wider bandwidth is required, a low Q filter is used to pass all of the information for a single channel.

Design of the single op amp bandpass filter can be simplified by making R_1 equal R_2 and C_1 equal C_2. Let's design a bandpass filter with a center frequency (f_r of 1500 *Hz*) and a bandwidth of 100 *Hz*. The first step in designing this filter is to find the value of Q. Then, choose a convenient value for R_1 and R_2 to allow the value of R_3 to be calculated. Let's choose $R_1 = R_2 = 10\ k\Omega$.

$$\text{because: } Q = \frac{f_r}{\text{BW}} \tag{6-21}$$

$$Q = \frac{1500\ Hz}{100\ Hz}$$

$$Q = 15$$

$$\text{so:}\quad 15 = .5\sqrt{\frac{R_3}{5\ k\Omega}} \quad \text{since } R_p = \tfrac{1}{2}R_1$$

$$30 = \sqrt{\frac{R_3}{5\ k\Omega}}$$

$$900 = \frac{R_3}{5\ k\Omega}$$

$$R_3 = 4.5\ M\Omega$$

Lastly, calculate a value of capacitance by rearranging the center frequency formula.

$$f_r = \frac{1}{2\pi\sqrt{R_pR_3}C} \quad \text{when } C = C_1 = C_2 \tag{6-22}$$

$$C = \frac{1}{2\pi\sqrt{R_pR_3}f_r} \tag{6-23}$$

$$C = \frac{1}{2\pi\sqrt{(5\ k)\,(4.5\ M)}\,1500}$$

$$C = \frac{1}{2\pi\,(150\ k)\,1500}$$

$$C = 700\ pF = C_1 = C_2$$

This is one of the few occasions where it is advisable to choose a resistance and calculate a capacitor value.

Topic Review 6-4

1. A ________ filter is used to pass a band of frequencies while rejecting frequencies either above or below that band.

2. ________ is the ability of a filter to pass a selected frequency and reject all other frequencies and is expressed as the quality of the filter, Q.

Answers:

1. bandpass
2. selectivity

6-5 Band-Reject (Notch) Filters

There are many applications where it is desirable to filter out a particular band of frequencies while passing all other frequencies. Some situations where this applies are: 60 *Hz* hum, small appliance noise in the home, noise caused by generators and motors in the work place, and anywhere that a particular frequency needs to be eliminated.

A band-reject (notch) or band-eliminator filter attenuates only a band of frequencies in the frequency spectrum, while passing all frequencies below and above the stopband.

The simplest means of achieving this is to sum the outputs of a low-pass and a high-pass filter with a summing amplifier. The response curve for such a filter is shown in **Figure 6-19**, and the actual circuit is shown in **Figure 6-20.**

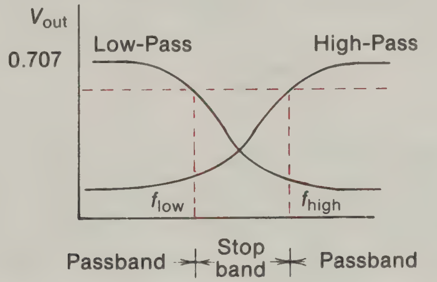


Figure 6-19. Three op amp notch filter response curve

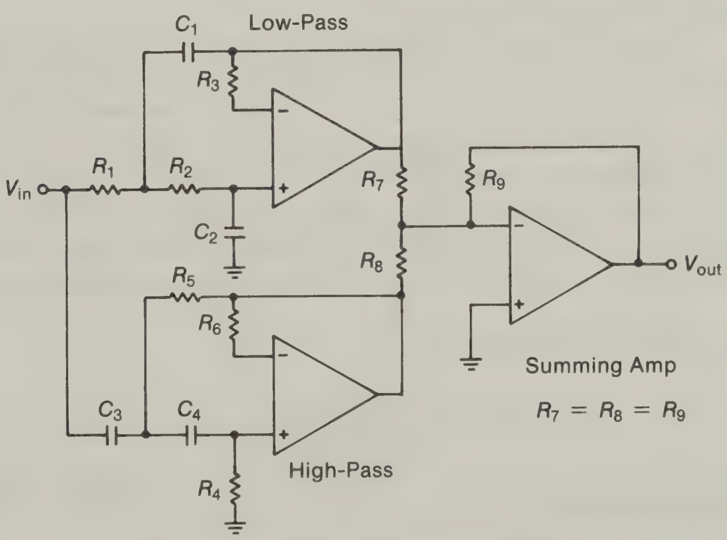


Figure 6-20. Three op amp notch filter

In this configuration, gain may be incorporated with the summing amp.

Circuit values are selected so that f_c, the cutoff frequency for the low-pass, occurs at a lower frequency than f_c for the high-pass. The f_c for the low-pass, becomes f_{low} for the filter; and f_c for the high-pass, becomes f_{high} for the filter. The bandwidth or stopband will be the distance (in hertz) between f_{low} and f_{high}. Notice that the band rejection occurs below the 0.707 point of the response curve, **Figure 6-19.**

The same formulas for Q and BW, used with the bandpass filter, apply to the notch filter.

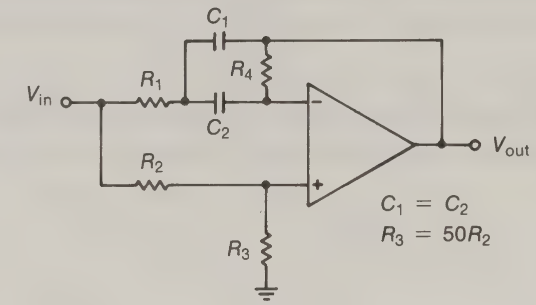


Figure 6-21. Single op amp notch filter

Figure 6-21 shows a single op amp notch filter. The input signal is applied to the noninverting input, through voltage divider R_2 and R_3. R_3 is generally made at least fifty times larger than R_2, which applies nearly all of the input signal voltage to the noninverting input of the op amp. This holds V_{out} at maximum until the input frequency is between f_{low} and f_{high}.

R_4 and C_2 form a high-pass filter whose f_c is the f_{low} of the notch filter. For frequencies up to f_{low}, C_2 blocks the input signal to the inverting input, causing it to have no effect on the output. As the input frequency increases above f_{low}, C_2 conducts more, applying more of the input signal to the inverting input. This will allow the inverting input's influence to be felt at the output, diminishing the output voltage.

R_1 and C_1 form a low-pass filter, where f_c is the f_{high} of the notch filter. For frequencies below f_{high}, C_1 blocks feedback current. As the input frequency increases above f_{high}, C_1 shunts current away from the inverting input, reducing its effect on the output.

f_r can be found by the formula:

$$f_r = \frac{1}{2\pi C\sqrt{R_1R_4}} \tag{6-24}$$

Q can be calculated by:

$$Q = .5\sqrt{\frac{R_4}{R_1}} \tag{6-25}$$

$$\text{where } C_1 = C_2$$

The values of X_{C_1} and X_{C_2} will allow the output to swing negative for only a small band of frequencies.

Let's design a notch filter to eliminate 60 Hz hum, with a bandwidth of 5 Hz. As with bandpass filters, choose a convenient value of R_1 and determine the quality (Q) of the filter. Let's choose $R_1 = 10\ k\Omega$.

$$Q = \frac{f_r}{\text{BW}} \tag{6-26}$$

$$Q = \frac{60}{5}$$

$$Q = 12$$

therefore:

$$12 = .5\sqrt{\frac{R_4}{10\ k\Omega}}$$

$$24 = \sqrt{\frac{R_4}{10\ k\Omega}}$$

$$576 = \frac{R_4}{10\ k\Omega}$$

$$R_4 = 5.7\ M\Omega$$

Next, calculate the value of C from the center frequency formula:

$$f_r = \frac{1}{2\pi C\sqrt{R_1 R_4}} \tag{6-27}$$

$$C = \frac{1}{2\pi\sqrt{(5.7\ M)\ (10\ k)}\ 60}$$

$$C = \frac{1}{2\pi\ (237\ k)\ 60}$$

$$C = 0.01\mu F = C_1 = C_2$$

Topic Review 6-5

1 The _______-_______ filter or notch filter attenuates only a band of frequencies in the frequency spectrum, while passing all frequencies above and below that band.

2. In **Figure 6-19**, the band rejection occurs below the ______ point of the response curve.

Answers:

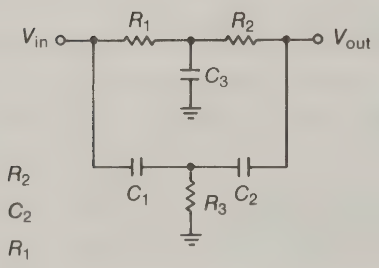
1. band-reject
2. 0.707

6-6 Twin-T Filters

Another popular filter circuit configuration is the twin-T circuit, shown in **Figure 6-22**. The twin-T is used in both bandpass and notch-type filters.

The component relationships stated in **Figure 6-22** are standard for the twin-T. The operation of the twin-T is fairly simple. At f_r, the twin-T network passes no current. The voltage in the upper-T is 180° out-of-phase with the lower-T and equal, thereby cancelling out the signal.

For frequencies lower than f_r, the upper-T (low-pass) will develop the output voltage across C_3. For frequencies above f_r, the lower-T (high-pass) will develop the output voltage across R_3. It is important that components be well matched when using the twin-T configuration, to insure good performance.



$R_1 = R_2$
$C_1 = C_2$
$2R_3 = R_1$
$2C_1 = C_3$

Figure 6-22. Twin-T network

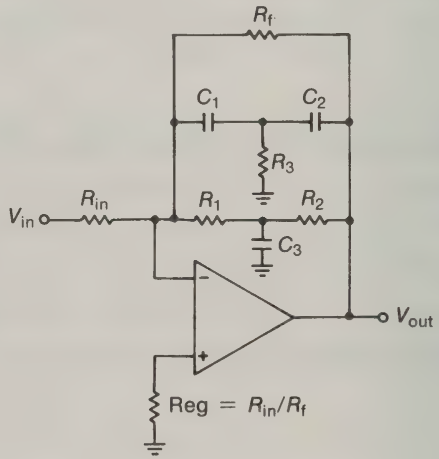


Figure 6-23. Twin-T bandpass filter

In **Figure 6-23** at f_r (null frequency) of the twin-T, no degenerative feedback is passed through the twin-T. The gain of the filter at f_r is established by:

$$V_{out} = -\frac{R_f}{R_{in}}(V_{in}) \qquad (6\text{-}28)$$

which is a simple inverting amplifier. As the frequency moves away from f_r in either direction, feedback will be applied to the inverting input through the appropriate T, causing the output to be diminished.

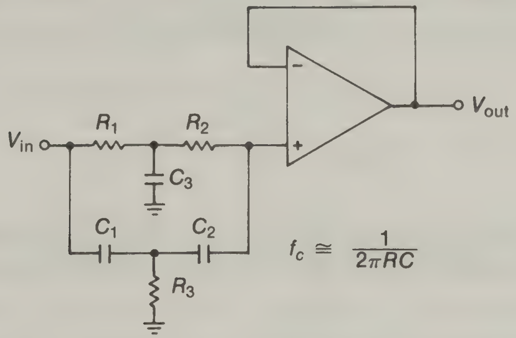

V_{in}
R_1
R_2
C_3
C_1
C_2
R_3
−
+
V_{out}
$f_c \cong \frac{1}{2\pi RC}$

Figure 6-24. Twin-T active notch filter

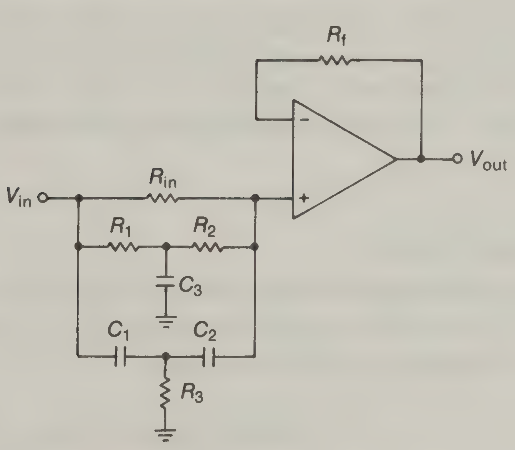

R_f
−
+
V_{out}
V_{in}
R_{in}
R_1
R_2
C_3
C_1
C_2
R_3

Figure 6-25. Twin-T notch filter with gain

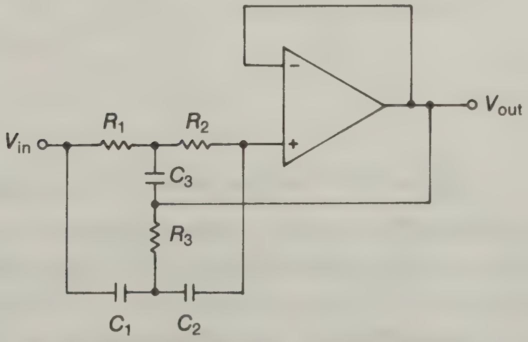

−
+
V_{out}
V_{in}
R_1
R_2
C_3
R_3
C_1
C_2

Figure 6-26. High-Q, twin-T notch filter

When using the twin-T as a notch filter as in **Figure 6-24**, the twin-T is placed in the input branch of the filter. The twin-T passes less current to the input of the op amp buffer or amplifier as the input frequency approaches f_r. At f_r the signal is completely removed from the input, which produces a very deep notch in the frequency response curve of the filters. In **Figure 6-25**, the output of the circuit at f_r is found by:

$$V_{\text{out}} = \left(\frac{R_f}{R_{\text{in}}} + 1\right) V_{\text{in}} \tag{6-29}$$

which is a simple noninverting amplifier. f_r or "null" frequency for any of the twin-T circuits shown, with suggested component relationships, is:

$$f_r = \frac{1}{2\pi R_1 C_1} \tag{6-30}$$

This relationship makes the design procedure for twin-T filters identical to the procedure for designing high and low-pass equal component filters. First, choose an appropriate capacitor value for C_1. Let $C_1 = C_2 = \frac{1}{2}C_3$. Next, calculate the value of R_1. Let $R_1 = R_2 = 2R_3$. Finally choose resistor values between $10k$ and $50k$ ohms for the gain resistors.

6-7 Multiple-Feedback Filters

A different approach to second-order, low, and high-pass filtering, is the multiple-feedback loop filter. These filters apply the input signal to the inverting terminal of the op amp and use an additional feedback path.

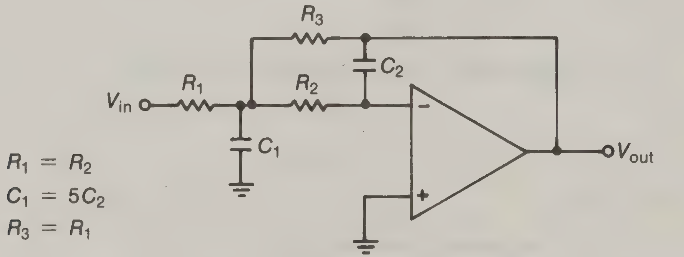


Figure 6-27. Multiple-feedback low-pass filter

As shown in **Figure 6-27**, R_1 and C_1 form a passive input filter, while R_2 and C_2 form the feedback filter. At frequencies below f_c, the input filter pre-filters the input signal, but the reactance of C_2 holds degenerative feedback to a minimum. This action allows maximum amplitude of the output signal in the filter's passband. For frequencies above f_c, the reactance of C_2 decreases, allowing more degenerative feedback to further attenuate the input signal. The f_c for this filter configuration, can be found by:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{6-31}$$

The circuit gain in the passband is determined by:

$$A_v = -\frac{R_3}{R_1} \tag{6-32}$$

In order to produce a Butterworth response, the gain should be held to one, so R_3 should equal R_1. The ratio of C_1 to C_2, for this type of filter, should be 5 to 1.

This filter can also be used to perform high-pass filtering by exchanging the resistive and capacitive elements from the low-pass filter. An example is as shown in **Figure 6-28**.

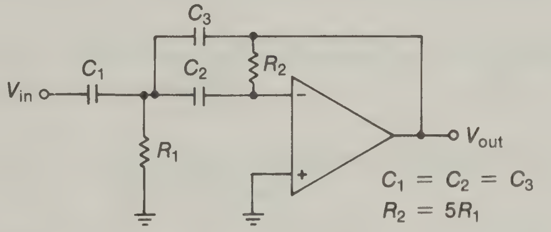


Figure 6-28. Multiple-feedback high-pass filter

The cutoff frequency is calculated by:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{6-33}$$

and passband gain is determined by:

$$A_v = \frac{C_3}{C_1} \tag{6-34}$$

Topic Review 6-7

1. ______ feedback filters combine the properties of ______-______ and high-pass filters for filtering action.

2. Cutoff frequency is found by the formula ______ in **Figure 6-28**.

Answers:

1. Multiple, second-order
2. $f_c = \dfrac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$

6-8 State-Variable Filters

State-variable filters are multiple-stage configurations which provide low-pass, high-pass, and bandpass filtering simultaneously. Multiple op amps are used to provide the separate outputs. These filters offer independent frequency and selectivity tuning, through the use of multiple feedback loops and variable resistors, to control damping. They have the disadvantage of being more sensitive to component aging and drift than other types of filters.

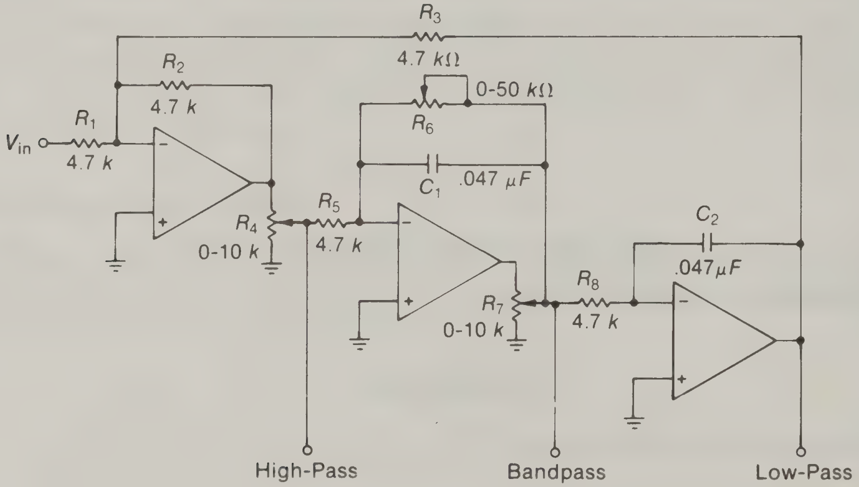


Figure 6-29. State-variable filter

The state-variable filter, in **Figure 6-29**, uses analog math techniques, rather than expanding passive *RC* filters, to provide the desired filtering. The circuit consists of a summing amplifier and two integrators, as shown in **Figure 6-29**. Resistors R_4 and R_7 are made variable to allow adjustment of the output frequencies, and R_6 is used to adjust the quality (Q) of the bandpass filter.

Design of the state-variable filter is simple, if $R_1 = R_2 = R_3$, $R_5 = R_8$, $R_4 = R_5$ and $R_6 = 10R_5$. Also, C_1 should equal C_2. The maximum frequency of operation is determined by:

$$f_{\max} = \frac{1}{2\pi R_5 C_1} \tag{6-35}$$

The minimum frequency of operation can be calculated by:

$$f_{\min} = \frac{1}{2\pi(R_4 + R_5)C_1} \tag{6-36}$$

6-9 Summary Points

1. There are four basic types of filters: low-pass, high-pass, bandpass, and band-reject.
2. Filter circuits are classified as either passive or active. Passive filters are constructed with resistors, capacitors and inductors. Active filters use transistors or op amps, along with resistors and capacitors, to filter signals.
3. Active filters have the advantages of no signal loss, easy adjustment, and electrical isolation between load and input.
4. Active filters have their drawbacks, such as a limited range of operating frequencies and the need for a power supply.
5. Rolloff is a term used to indicate how much a filter attenuates an input signal as the signal moves into the stopband of the filter.
6. A first-order filter has a rolloff of $-20\ dB/$decade. A decade is a tenfold increase or decrease in frequency, from the cutoff frequency, f_c.
7. Cutoff, f_c, is the frequency at which the output response falls off to 70.7% of the maximum amplitude on a response curve.
8. A Butterworth response indicates that the gain of the filter will be constant in the passband of the response curve.
9. The order of a filter indicates the rate at which the filter response will rolloff. The rolloff is the product of the filters order, times the rolloff of a first-order filter. A second-order filter will rolloff at a rate of $2 \times -20\ dB/$decade or $-40\ dB/$decade.
10. Filters with orders higher than second are constructed by cascading lower order filters.

11. High and low-pass second-order filters can be constructed by scaling the input and feedback element by a ratio of 2 to 1. They may also be constructed by making all of the frequency determining components equal, and making the passband gain 1.5.

12. Bandpass filters pass a band of frequencies in the center of the frequency spectrum while rejecting the lower and higher frequencies.

13. Bandpass filters are divided into wide bandpass filters (BW = 10% of f_r) and narrow bandpass filters (BW = 10% of f_r).

14. Quality is an indication of the filters selectivity and is calculated by dividing the center frequency, f_r, by the bandwidth.

15. Notch filters pass all frequencies in the spectrum, except a selected band in the middle of the spectrum.

16. Twin-T filters are an easy-to-design configuration, which can be used as either a bandpass or a band-reject filter.

17. At the "null" frequency of the twin-T, no current passes through the filter.

18. Multiple-feedback filters provide high or low-pass second-order filtering, by using the inverting input of the op amp and multiple-feedback loops.

19. State-variable filters are multiple-feedback, multiple op amp configurations; which provide low-pass, high-pass, and bandpass filtering simultaneously.

20. Filter design is usually performed by first choosing capacitor values and then calculating resistance values.

6-10 Chapter Progress Evaluation

1. What type of filter has a nearly constant output response from DC to cutoff?

2. What type of filter will pass a band of frequencies in the middle of the frequency spectrum, while rejecting the higher and lower ends of the frequency spectrum?

3. Identify the type of filter which produces the response curve shown in **Figure 6-6**.

4. The group of frequencies that a filter allows to pass through it unaffected is termed the filters:

5. The gradual increase in attenuation of the signal as frequency increases is called:

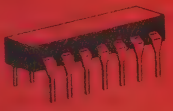
6. A decade is a frequency increase of times ten above:

7. Find the cutoff frequency, f_c, of the second-order low-pass filter of **Figure 6-4**, if R_1 equals 10 $k\Omega$, C_1 equals 0.2 μF. R_1 equals R_2 and C_1 equals $2C_2$.

8. The third-order high-pass filter of **Figure 6-10** has the following component values: R_4 equals 20 $k\Omega$, C_1 equals 0.01 uF, and C_1 equals C_2 equals C_3. Find f_c

9. Quality or Q of a filter is inversely proportional to:

10. Find the Q of the circuit in **Figure 6-18**, if bandwidth equals 150 Hz and center frequency, f_r, equals 2500 Hz.



Chapter 7

Norton Amplifiers

Objectives

Upon completion of this chapter, you should be able to do the following:

- Explain the operation of the internal stages of the Norton amplifier
- Describe inverting and noninverting operations
- List alternative methods of biasing
- Describe the operation and characteristics of the Norton differential amplifier
- List the applications of Norton amplifiers

7-1 Introduction

Another form of the operational amplifier is the *Norton amplifier*. Originally, the Norton amplifier was developed to add some features not possessed by standard operational amplifiers, such as a single power supply operation and a lower operating cost.

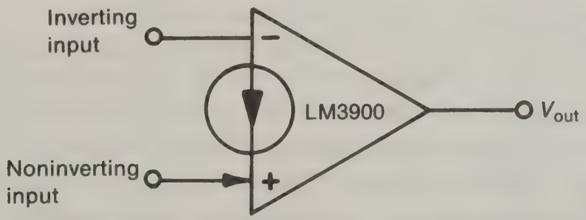


Figure 7-1. The Norton amplifier schematic symbol

Shown in **Figure 7-1** is the schematic symbol of a Norton amplifier. Notice that it is very similar to the symbol for a standard operational amplifier. Notice also that the symbol for a current source is placed between the two inputs. This indicates the difference between the Norton amplifier and conventional operational amplifiers.

Standard op amps employ a differential amplifier and operate on a difference voltage principle. However, the Norton amplifier operates on a difference current principle and uses a current mirror to provide a noninverting input. It is therefore called a current differencing amplifier, or CDA.

Internally, the Norton amplifier is fairly simple to analyze. Basically, it has only three stages: the constant current sources (which have already been discussed), the current mirror input stage, and the high gain amplifier stage.

The Current Mirror: By definition, a *current mirror* is any circuit where the output current is forced to equal the input current. The constant current sources established in the discussion of the 741 op amp are prime examples. In the Norton amplifier, a current mirror is used by the current differencing input stage at the noninverting terminal (+). The current input stage is shown in **Figure 7-2.** The current mirror consists of transistors Q_* and Q_6. Q_* provides a constant voltage source and temperature stabilization for Q_6.

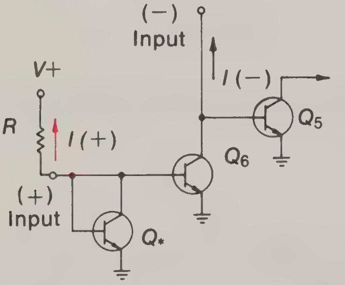


Figure 7-2. The Norton amplifier input stage
Courtesy National Semiconductor Corp.

Current $I+$ can be thought of as the collector current of Q_*. Actually, there are three IC currents to consider: I_{C*}; I_{B*}; and I_{B6}. However, the collector current is so much larger than the two base currents ($I_C = I_B \times \beta$), that for all practical purposes, $I+ = I_{C*}$, which is determined by $V+$ and R. Since the bases of Q_* and Q_6 are tied together, the same voltage (approximately +0.6 because of the base-emitter junction) is applied to the bases of both transistors. Therefore, both transistors should have identical base currents. And since they were fabricated by the monolithic process, their collector currents should also be equal. Since I_{CQ6} is much larger than the current flowing into the base of Q_5, we can state that $I+$ is approximately equal to $I-$ at quiesence (no input). This condition of zero current differential is very similar to the zero voltage differential present at the inputs of the 741 op amp.

The input to the high gain amplifier stage, which follows this particular stage, is taken from the collector of transistor Q_5, which also provides the inverting input.

Since both Q_5 and Q_6 are wired in common emitter fashion, any signal applied to their bases is inverted at their collectors. Signals placed on the base of Q_5 are applied to the high gain amplifier stage in inverted form, so the base of Q_5 is used as the inverting input. Signals placed on the base of Q_6 are inverted and inverted again by Q_5, so the base of Q_6 is used to provide the noninverting input.

It should also be noted at this point that the two inputs are biased to always be at a potential of approximately +0.6 volts (or the voltage drop of one forward biased base-emitter junction) above ground. This voltage drop is termed V_{BE}, and because of V_{BE}, the inputs must never be connected directly to a voltage source. **Appropriate current limiting resistors must be used on both inputs. If any level other than +6 VDC is measured at the inputs, the input diodes have been destroyed and the device is useless.**

The Gain Stage: A simplified version of the Norton amplifier's *gain stage* is shown in **Figure 7-3**. Notice that transistor Q_5 is shared by the input stage and the gain stage.

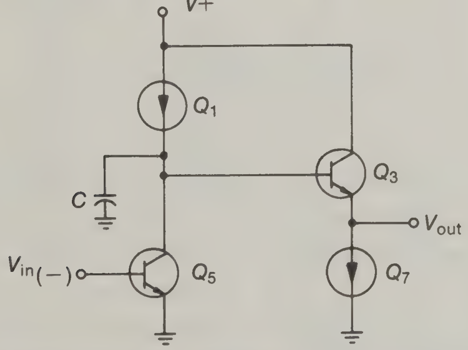


Figure 7-3. A simplified Norton gain stage

The gain of a common emitter amplifier (Q_5) is determined by the collector resistance, divided by the emitter resistance. Approximately the same current flows through R_C as flows through R_E. Therefore, the ratio of voltages, which is gain, are equal to the ratio of resistance. Since the impedance of a constant current source is extremely high (nearly infinite), the presence of constant current source Q_1 , in the collector circuit of Q_5, gives the amplifier very high gain, especially when compared to the very low (nearly zero) impedance of the emitter. Typically, the gain of this configuration is about 2800, or +60 to +70 *dB*.

Remember that the output impedance of an op amp should be as low as possible. This is achieved by wiring transistor Q_3 as an emitter follower, with constant current source Q_7 as a load. This configuration allows the op amp's load to be isolated from the high output impedance of the common emitter amplifier.

The use of constant current source Q_7, in the emitter follower, allows low current drain on the power supply, because of its high impedance. And since it is a constant current source, the quiescent emitter current is very constant, even if the power supply ($V+$) varies. This is an important feature of Norton amplifiers.

Internal frequency compensation is provided by capacitor *C*, which establishes the frequency response of the op amp. The unity gain frequency of the Norton amplifier is 2.5 *MHz*.

The complete Norton amplifier gain stage is made superior to this simple gain stage by the addition of a lateral pair, to increase the current gain of the op amp. The complete Norton amplifier (in this case the LM3900) gain stage is shown in **Figure 7-4**.

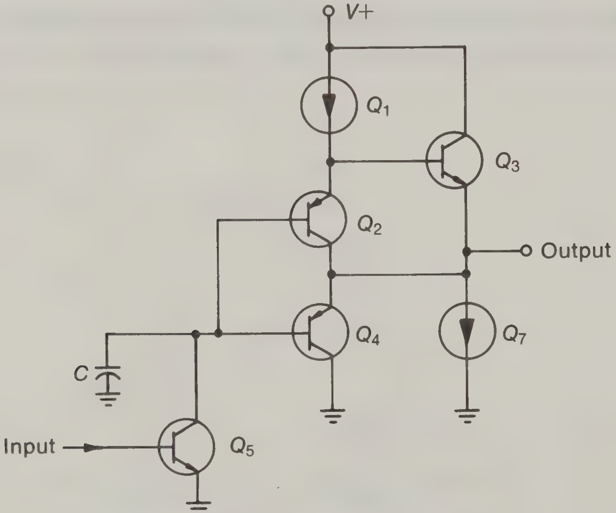


Figure 7-4. The LM3900 gain stage
Courtesy National Semiconductor Corp.

The addition of the lateral pair of PNP transistors, Q_2 and Q_4, does not change the input or output voltage characteristics of the op amp. This is because they are wired as emitter followers, which do not amplify, but do increase the current gain of the circuit, thereby improving small signal amplification. Additionally, PNP transistor Q_4 is in parallel with constant current source Q_7. Since the impedance of Q_4 is much lower than the impedance of Q_7, this combination allows the output to *sink* more current than if Q_7 were alone. **Sinking more current simply means the output current swing is increased, allowing the op amp output to drive more devices.**

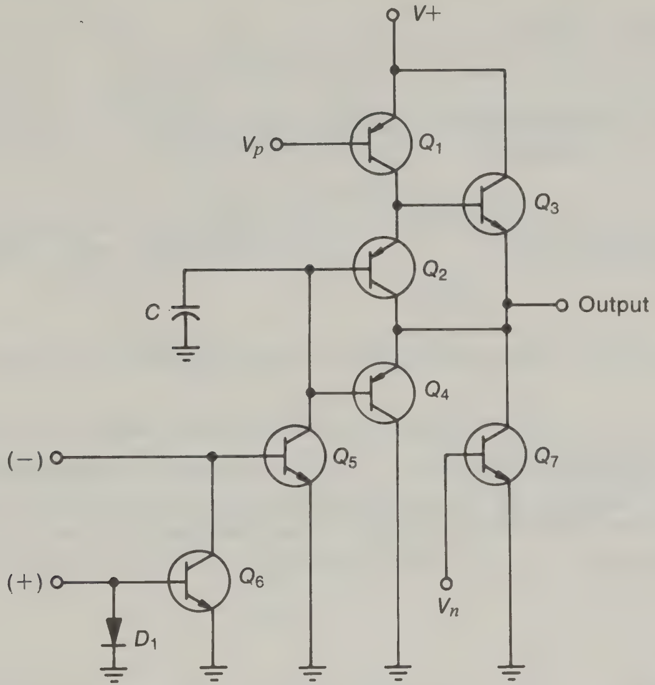


Figure 7-5. LM3900 schematic diagram
Courtesy National Semiconductor Corp.

The full schematic of the Norton amplifier is shown in **Figure 7-5**. Notice that transistor Q_* has been replaced by a diode symbol (D_1), and that constant current output transistors are shown instead of constant current sources for Q_1 and Q_7. This is done because the Norton amplifier is manufactured with four amps on a chip (quad), and the identical op amps share the constant voltage reference (which feeds V_p and V_n) of the constant current sources.

There are several advantages to the Norton amplifier design: it operates from a single power supply, and over a wide range of supply voltages; the circuit maintains stable operating characteristics, even if the power supply varies. The Norton amplifier can be used in most op amp applications, and interfaces easily with TTL and CMOS logic families; so it finds its way into many digital interface devices. The Norton amplifier can also function with signal voltages larger than $V+$, as long as large enough series resistors are used on the inputs.

There are also some disadvantages to the Norton amplifier. Some care must be taken to ensure that sufficient input resistance is used to limit the input current below 20 mA DC, because the chip can be very easily destroyed. Additionally, the Norton amplifier does not have extremely high performance characteristics (gain) like those possessed by conventional op amps, and is not suitable for ultra-low noise applications.

Topic Review 7-1

1. By definition, a current mirror is any circuit where the ______ current is forced to equal the ______ current.
2. The two inputs to a typical Norton amplifier, with zero current differential, are biased at approximately ______ volts above ground. This voltage drop is termed V_{BE}.
3. The gain stage of a Norton amplifier is typically about 2800, or + ______ *dB*.
4. In **Figure 7-3**, internal frequency compensation is provided by ______ . This limits the unity gain frequency of the Norton amplifier to approximately 2.5 *MHz*.
5. Along with many of the advantages of the Norton amplifier, a disadvantage is the necessity of input ______ to limit the current to below 20 *mA*.

Answers:

1. output, input
2. +0.6 VDC
3. 65
4. capacitor *C*
5. resistors

7-2 Linear Norton Amplifier Operations

The Norton amplifier was originally developed as a single supply AC amplifier. **The question is: How do you process AC signals with a DC device that operates between a single supply voltage and ground? The answer: Set the output to some quiescent DC voltage and let the AC signal swing positive and negative with respect to the DC voltage level, instead of ground.** This practice is termed "biasing." The configuration for conventional Norton amplifier biasing is shown in **Figure 7-6**.

Typically (but not always), the Norton amplifier output is biased to one-half of $V+$. This allows the AC output signal to swing equally above and below the DC level.

Current from the noninverting input is determined by the values of $V+$ and R_B.

$$I+ = \frac{V+ - V_{BE}}{R_b} \tag{7-1}$$

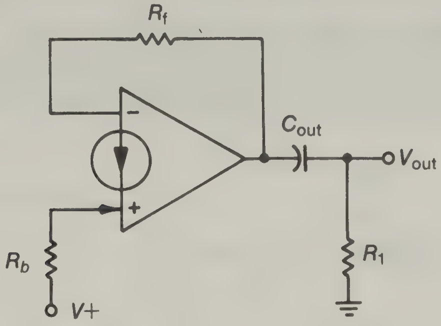


Figure 7-6. Conventional biasing circuit

Voltage drop V_{BE} is small compared to $V+$, so V_{BE} may be dropped to simplify calculations without effecting the amplifier's operation. This allows the equation to be simplified to:

$$I+ = \frac{V+}{R_b} \tag{7-2}$$

The action of the current mirror ensures that $I-$ equals $I+$. $I-$ flows out of the inverting input, through feedback resistor R_f, into the output terminal, and through Q_3 (in the previous gain stage) to $V+$. Disregarding V_{BE}, the DC output voltage is found from:

$$V_{\text{out(DC)}} = R_f \times I- \tag{7-3}$$

Since $I+$ equals $I-$, substituting from equation (7-2), we can say:

$$V_{\text{out(DC)}} = R_f \left(\frac{V+}{R_b}\right) \tag{7-4}$$

Since the Norton is usually, but not always, biased to one-half of $V+$:

$$V_{\text{out(DC)}} = \frac{1}{2}\ V+ \tag{7-5}$$

$$\frac{R_f}{R_b}\ (V+) = \frac{1}{2}\ (V+) \tag{7-6}$$

$$R_f = \frac{1}{2} \tag{7-7}$$

$$2R_f = R_b \tag{7-8}$$

R_b must be twice as large as R_f, to bias the output to one-half of $V+$.

There may be occasions when it is desirable to bias the output to some value other than one-half of $V+$. If we wish to bias the output to some other level, say one-fourth of $V+$, we simply insert the desired level into the previous formula.

$$V_{\text{out(DC)}} = \frac{1}{4} V+$$

$$\frac{R_f}{R_b}(V+) = \frac{1}{4} V+$$

$$\frac{R_f}{R_b} = \frac{1}{4}$$

$$4\,R_f = R_b$$

This relationship biases the output to one-fourth of $V+$, allowing an AC output to swing three times more positive than it can negative.

Topic Review 7-2

1. The linear Norton amplifier operates between a single supply voltage and ______. This allows the amplifier to process AC signals.

2. Typically (but not always), the Norton amplifier output is biased to one-half of ______. This allows the AC output signal to swing equally above and below the DC level.

3. Also, ______ must be twice as large as R_f to bias the output to $\frac{1}{2}$ $V+$.

4. If we wish to bias at $\frac{1}{4}$ $V+$, then $V_{\text{out(DC)}} =$ ______.

5. And, R_b is now ______ times larger than R_f, or $4R_f = R_b$.

Answers:

1. ground
2. $V+$
3. R_b
4. $\frac{1}{4}$ $V+$
5. 4

7-3 Inverting Amplifier

The Norton can be configured as an *inverting* amplifier by applying a signal voltage to the inverting input, through the input network, as shown in **Figure 7-7**.

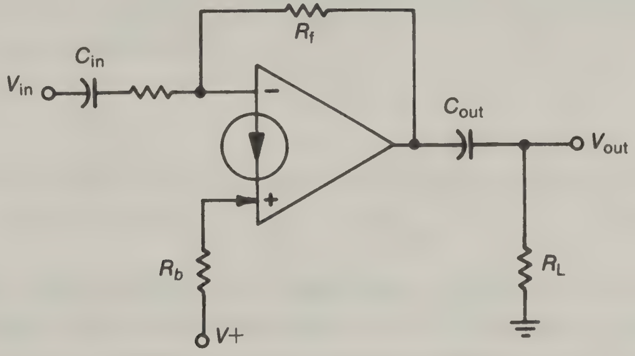


Figure 7-7. The inverting amplifier

Bias current flows from the noninverting terminal and the inverting terminal. Capacitors C_{in} and C_{out} charge up and prevent the DC bias current from flowing out of the input or the output. AC signal currents are added to, or subtracted from, the bias current through C_{in} and R_{in}.

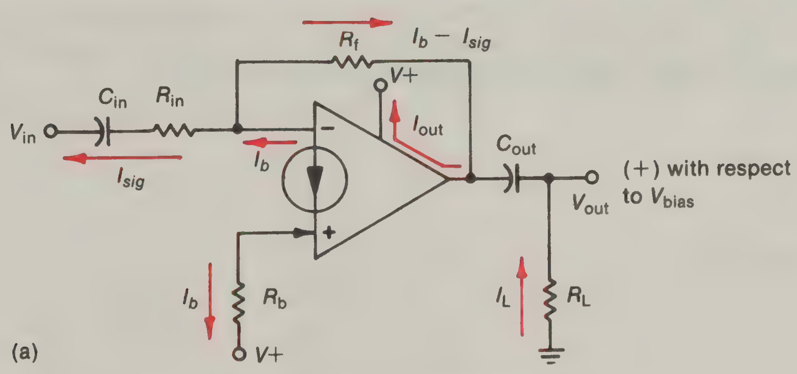


Figure 7-8. Inverting amplifier current flow

The operation of the circuit can be seen clearly in **Figure 7-8a**, by examining the currents present at the inverting terminal. Bias current flows out of the inverting current, due to the current mirror. When a positive going AC signal is applied to the input signal, current flows out of the input through R_{in}. Kirchhoff's current law states that the current entering a node must equal the current leaving the node. From this, we can see that the current through the feedback loop must be the bias current minus the signal current, since the current coming out of the inverting input is held constant at I_b by the current mirror.

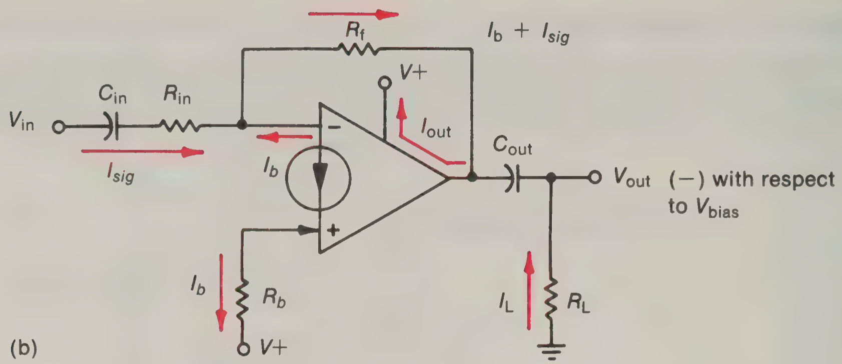


Figure 7-8. (continued)

Conversely, when a negative AC signal is applied to the input, as shown in **Figure 7-8b**, signal current flows into the input through R_{in}. Examining the node once again, we see that the feedback current is the signal current added to the bias current.

Recall that the output voltage is determined by the amount of current flowing through the feedback resistor. So, as the input signal swings further negative, more current flows through the feedback resistor and the output voltage swings positive with respect to the DC bias voltage ($V_{out(DC)}$). Since the bias current through R_f sets the reference level, the current through R_f, due to the input signal, is equal and opposite to the input current. Gain is determined by the output voltage, divided by the input voltage. So, gain of the amplifier is determined by:

$$A_V = \frac{V_{out}}{V_{in}} \tag{7-9}$$

therefore:

$$A_V = \frac{-I_{sig}(R_f)}{I_{sig}R_{in}} \tag{7-10}$$

$$A_V = -\frac{R_f}{R_{in}} \tag{7-11}$$

The input impedance is determined by the reactance of the input capacitor, X_{cin}, and the value of R_{in}.

$$Z_{in} = \sqrt{X_{Cin}{}^2 + R_{in}{}^2} \tag{7-12}$$

The effects of the capacitor on the input impedance can be minimized by choosing a capacitor value that will produce a reactance that is less than one-tenth of C_{in} at the circuits lowest frequency of operation.

$$X_{C\text{in}} = \frac{1}{2\pi F C_{\text{in}}} \quad \text{or} \quad X_{C\text{in}} = \frac{1}{10} Z_{\text{in}} \tag{7-13}$$

This allows us to ignore the effects of X_C and simply call R_{in} the input impedance.

Topic Review 7-3

1. In the Norton inverting amplifier of **Figure 7-8a**, bias current, I_b, flows out of the inverting input, due to the action of the ______ ______.

2. Therefore, the current through the feedback loop, R_f, equals ______ minus ______, since current coming out of the inverting input is held constant at I_b by the current mirror.

3. Gain is determined by the ______ voltage, divided by the ______ voltage, in the Norton inverting amplifier.

4. Also, $A_V =$ ______ or ______, for the Norton inverting configuration in **Figure 7-8a**.

5. Providing $X_{C\text{in}} =$ ______ Z_{in} at the circuit's lowest frequency of operation, then for all practical purposes, $X_{C\text{in}}$ can be ignored, and $R_{\text{in}} = Z_{\text{in}}$.

Answers:

1. current
   mirror
2. I_b,
   I_{sig}
3. output,
   input
4. $\frac{-R_f}{R_{\text{in}}}, \frac{V_{\text{out}}}{V_{\text{in}}}$
5. $\frac{1}{10}$

7-4 Noninverting Amplifier

The fundamentals of the *Norton noninverting amplifier* are very similar to the inverting amplifier. The DC biasing is identical; in order to establish the quiescent output voltage at one-half of $V+$, resistor R_b must be twice as large as R_f. Also, the assumptions made about the inverting amplifier, concerning the size of the input capacitor and input impedance, apply to the Norton noninverting amplifier as well.

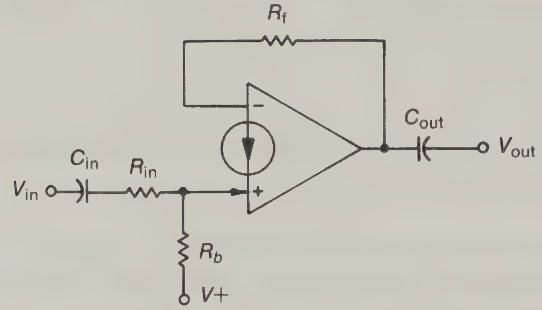


Figure 7-9. The noninverting amplifier

Examining the noninverting terminal shown in **Figure 7-9**, we see that the bias current flows out of the terminal, through R_b to $V+$ (once again, we are referring to electron flow, negative to positive). A positive going signal voltage applied to the input causes signal current to also flow out of the noninverting terminal, through R_{in} to V_{in}. The current mirror forces the current coming out of the inverting terminal to equal the current flowing out of the noninverting terminal.

$$I+ = I- \tag{7-14}$$

For a positive going signal, the noninverting current is the sum of the bias current and the signal current.

$$I(+) = I_b + I_{sig} \tag{7-15}$$

For a negative going signal, the signal current flows into the noninverting terminal. So, the noninverting terminal current is the bias current minus the signal current.

$$\mathrm{I}+ = I_b - I_{sig} \tag{7-16}$$

When a positive signal is applied to the input, $I+$ increases, and therefore $I-$ increases. As more current flows through the feedback resistor, the output voltage swings positive with respect to the bias level.

Likewise, a negative input signal causes the output voltage to swing negative with respect to the bias level. Therefore, there is no inversion of signal phase. From the gain formula:

$$A_v = \frac{V_{out}}{V_{in}} \tag{7-17}$$

Substituting Ohm's law for V_{out} and V_{in}:

$$V_{in} = I_{in}(R_{in}) \tag{7-18}$$

and:

$$V_{out} = I_f(R_f) \tag{7-19}$$

Disregarding I_b, since it establishes the reference level:

$$I_f = I_{in} \tag{7-20}$$

therefore:

$$A_v = \frac{I_{in}(R_f)}{I_{in}(R_{in})} \tag{7-21}$$

$$A_v = \frac{R_f}{R_{in}} \tag{7-22}$$

The design formulas for the inverting amplifier and the noninverting amplifier are identical, except for the (−) sign in the inverting amplifier gain formula. The (−) sign simply indicates phase inversion. Therefore, the design procedures are identical for both types of amplifiers.

As a practical example, let's design a Norton amplifier to given specifications.

Given: Input Impedance, $Z_{in} = 100\ k\Omega$
Voltage Gain, $A_v = 10$
Supply Voltage, $V+ = 12$ VDC
Output Voltage, $V_{out} = \frac{1}{2} V+$

Find: a) Feedback Resistor, R_f
b) Bias Resistor, R_b
c) Input Coupling Capacitor, C_{in}

Assume $R_{in} = Z_{in} = 100\ k\Omega$, since $X_{C_{in}}$ is very small.

If $X_{C_{in}} = \frac{1}{10} R_{in}$ at 1000 Hz

then: $X_{C_{in}} = 10\ k\Omega$

Next, find C_{in}.

$C_{in} = 0.016\ \mu F$ from:

$$X_{C_{in}} = \frac{1}{2\pi f C_{in}}$$

Next, find R_f.

$R_f = A_v \times R_{in} = 1\ M\Omega$ from:

$$A_v = \frac{R_f}{R_{in}}$$

Then, find R_b.

$$R_b = 2\ R_f \text{(to bias at } \frac{1}{2}\ V+)$$

therefore: $R_B = 2\ M\Omega$

All of the values necessary for designing a Norton amplifier, with a gain of 10, have been calculated.

Topic Review 7-4

1. In the noninverting Norton amplifier, resistor R_b must be ______ as large as R_f, in order to establish the quiescent output voltage at one-half of $V+$.
2. For a positive going input signal, as V_{in} swings more positive, V_{out} swings more ______ .
3. For a negative going input signal, as V_{in} swings more positive, V_{out} swings more ______ . Therefore, there is no input signal phase inversion at the output.
4. A_V, of the noninverting Norton amplifier, equals ______ or ______ .
5. As with the inverting Norton amplifier, $R_{in} = Z_{in}$, providing $X_C =$ ______ Z_{in} at the circuit's lowest frequency of operation.

Answers

1. twice
2. positive
3. negative
4. $\frac{V_{out}}{V_{in}}$,

$$\frac{R_f}{R_{in}}$$

5. $\frac{1}{10}$

7-5 Alternative Methods of Biasing

Since the Norton amplifier was originally developed as an AC amplifier, its use as a DC amplifier tends to make the circuitry around the amplifier somewhat more complicated. Also, the Norton amplifier is not well suited to low noise applications.

These drawbacks tend to limit the use of the Norton amplifier in these applications. However, there are exceptions. When circuits with high values of signal voltage are used, the Norton amplifier is best suited for the job. So, alternative methods of *biasing* have been developed to enhance the qualities of the Norton amplifier in these situations.

"NV_{BE}" biasing is used to improve the low noise performance of the Norton amplifier. This is accomplished by grounding the noninverting input, thereby defeating the current mirror and reducing the Norton amplifier to a simple high gain amplifier.

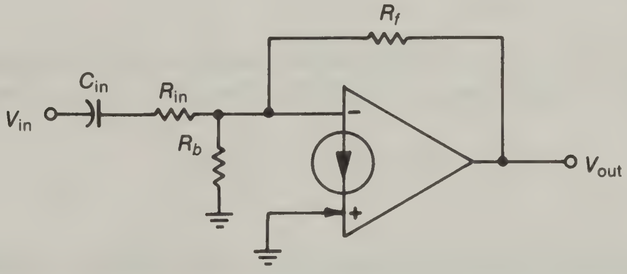


Figure 7-10. NV_{BE} biasing

In **Figure 7-10**, the DC bias current is caused to flow through R_b, because of V_{BE} (+0.6 volts). This current must flow through R_f to the output establishing the DC output voltage. Calculating the DC output voltage is a simple matter of rearranging the general voltage divider formula.

$$V_{ref} = \frac{R_2}{R_1 + R_2}(V+) \qquad (7\text{-}23)$$

Applying the voltage divider formula to the amplifier we get:

$$V_{BE} = \frac{R_b}{R_b + R_f}(V_{\text{out(DC)}}) \qquad (7\text{-}24)$$

$$V_{BE} = \frac{R_b}{R_b} + \frac{R_b}{R_f}\ (V_{\text{out(DC)}}) \qquad (7\text{-}25)$$

$$V_{BE} = 1 + \frac{R_b}{R_f}(V_{\text{out(DC)}}) \qquad (7\text{-}26)$$

$$\frac{V_{BE}}{V_{\text{out(DC)}}} = \frac{R_b}{R_f} + 1 \qquad (7\text{-}27)$$

Inverting both sides:

$$\frac{V_{\text{out(DC)}}}{V_{BE}} = \frac{R_f}{R_b} + 1 \qquad (7\text{-}28)$$

$$V_{\text{out(DC)}} = \frac{R_f}{R_b} + 1\ (V_{BE}) \qquad (7\text{-}29)$$

The gain of the circuit is established by the ratio of R_f to R_{in}.

$$A_v = -\frac{R_f}{R_{\text{in}}} \qquad (7\text{-}30)$$

The input impedance of the circuit can be called R_{in}, if the capacitive reactance of the input capacitor is less than $\frac{1}{10}$ of Z_{in} at the lowest operating frequency.

$$Z_{\text{in}} = R_{\text{in}} \quad (\text{if } X_c < \frac{1}{10} Z_{\text{in}}) \qquad (7\text{-}31)$$

Common mode biasing is employed to allow the Norton amplifier to accept input voltages below V_{BE} for DC applications. Common mode biasing is achieved by constructing equal resistor networks between $V+$ and the amplifier's inputs.

Common mode biasing is always constructed around an existing circuit. **Figure 7-11a** shows common mode biasing added to a noninverting Norton comparator. The biasing allows the output to be zero for an input of zero. It also allows negative values of input voltage and reference voltage to be used with the comparator. Common mode biasing is a particularly valuable tool with Norton comparators, but **Figure 7-11b** shows that constructing equal resistor networks around circuits such as the noninverting amplifier can become somewhat complicated.

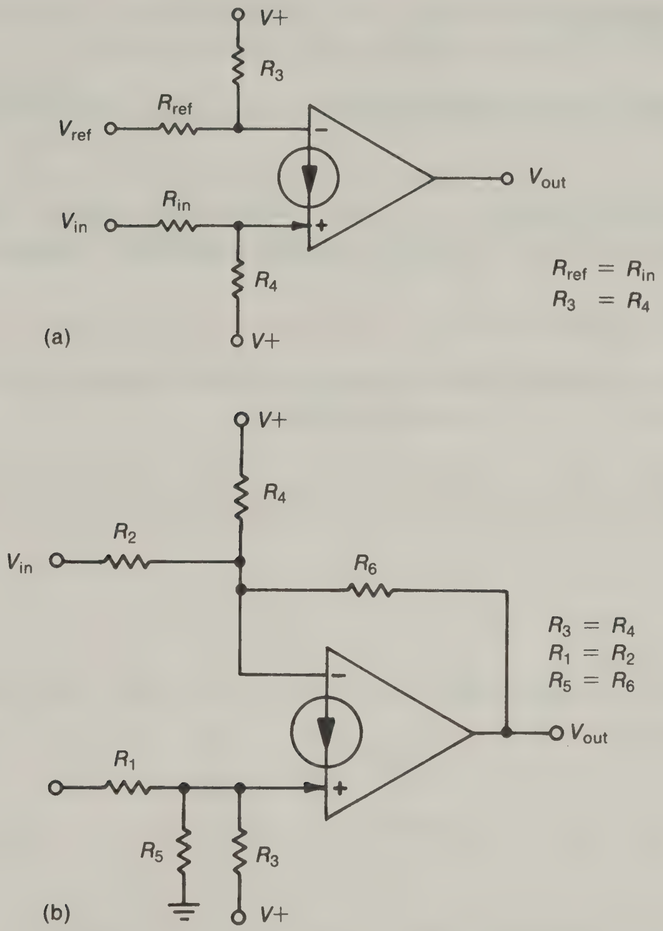

V+
R3
Rref
Vref
Vout
Rin
Vin
R4
V+
Rref = Rin
R3 = R4
(a)
V+
R4
R2
Vin
R6
R3 = R4
R1 = R2
R5 = R6
Vout
R1
R5
R3
(b)
V+

Figure 7-11. Common mode biasing

The component relationships, shown in **Figure 7-11b**, form identical resistor networks between the two inputs and $V+$. Since the inverting input current ($I-$) must be equal to noninverting current ($I+$), a potential of zero volts at the input causes the output to bias at zero volts. Both inputs are held at V_{BE}, allowing the two voltage dividers to determine the output voltage. Gain is established by the ratio of:

$$A_v = \frac{R_6}{R_1}$$

It should be noted that this configuration is usually avoided because of its complexity. When this type of network is needed, it becomes apparent that the general purpose 710 op amp can do a better job.

Topic Review 7-5

1. NV_{BE} biasing is used to improve the ______ ______ performance of the Norton amplifier.
2. This is accomplished by ______ the noninverting input, defeating the current mirror, and reducing the Norton amplifier to a simple high-gain amplifier.
3. Essentially, $V_{\text{out(DC)}}$ ______.
4. Since the noninverting input is grounded when biasing is in the NV_{BE} mode of operation, $A_V =$ ______, using R_f and R_{in}.
5. Once again $\_\_{}_{\text{in}} = \_\_{}_{\text{in}}$, providing $X_{C\text{in}} = \frac{1}{10} Z_{\text{in}}$ at the circuits lowest operating frequency.

Answers:

1. low noise
2. grounding
3. $\left(\frac{R_f}{R_b} + 1\right)(V_{BE})$
4. $\frac{R_f}{R_{\text{in}}}$
5. R,
   Z

7-6 Differential Amplifier

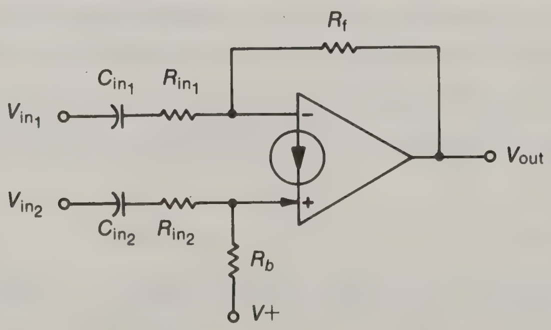


Figure 7-12. The differential amplifier

The Norton amplifier can be configured as a *differential* voltage amplifier as shown in **Figure 7-12**, by combining the characteristics of the inverting and noninverting Norton amplifiers.

The output of the differential amplifier can be determined by analyzing each input and combining the results.

The DC bias is established by resistors R_b and R_f.

$$R_b = 2R_f \text{ when } V_{out(DC)} = \frac{1}{2} V+ \tag{7-32}$$

The voltage gain, due to the inverting input, is determined by the ratio of R_f to R_{in_1} (inverted).

$$A_v- = -\frac{R_f}{R_{in_1}} \tag{7-33}$$

The voltage gain, due to the noninverting input, is determined by the ratio of R_f to R_{in_2}.

$$A_v+ = \frac{R_f}{R_{in_2}} \tag{7-34}$$

If equal values of input resistance are used, the output voltage is simply:

$$V_{out} = \frac{R_f}{R_{in}} (V_{in_2} = V_{in_1}) \tag{7-35}$$

For cases where $R_f = R_{in}$, the output can be determined simply by:

$$V_{out} = (V_{in_2} - V_{in_1}) \tag{7-36}$$

The same procedure given for choosing the input capacitors for inverting and noninverting amplifiers should be followed with this configuration. This allows us to use R_{in_1} as the input impedance for the inverting input, and R_{in_2} as the input impedance for the noninverting input, which makes the differential input impedance equal to:

$$Z_{in\,(diff)} = R_{in_1} + R_{in_2} \tag{7-37}$$

Topic Review 7-6

1. The Norton differential amplifier combines the characteristics of the ______ and ______ Norton amplifiers.

2. Voltage gain, $-A_V$, due to the inverting input, is determined by the ratio of ______ to ______ .

3. Voltage gain, $+A_V$, due to the noninverting input, is determined by the ratio of ______ to ______.

4. If equal values of input resistance are used, the output voltage of a Norton differential amplifier is simply: V_{out} = ______.

5. To allow the Norton amplifier to accept input voltages below V_{BE} for DC applications, ______ ______ biasing is used. This type of biasing is achieved by constructing equal resistor networks between $V+$ and the amplifier's inputs.

Answers:

1. inverting,
   noninverting
2. R_f,
   R_{in}
3. R_f
   $(V_{in2} - V_{in1})$
4. $\dfrac{R_f}{R_{in}}$
5. common mode

7-7 Comparators

The Norton amplifier is simple to implement as a *comparator*; and since its input voltage is virtually unlimited, provided sufficient series input resistance is used, *Norton comparators* are employed in many applications where conventional op amps are impractical.

With Norton comparators, the reference voltage is established by a resistive voltage divider, just as it was with the 741 op amp. The resistor values used in the voltage divider should follow the guidelines given in the section on conventional voltage level detectors. Typically, $R_1 + R_2$ should equal one-tenth to one one-hundredth the value of the input resistor. The same value of series resistance must be used for both inputs.

The Norton amplifier may be configured as an inverting comparator (Figure 7-13a) or a noninverting comparator (Figure 7-13b). The value of V_{ref} can be established at any level greater than V_{BE} (approximately +0.6 volts).

Looking at **Figure 7-13a**, the operation of a comparator is quite simple. If I_{in}, the current through R_{in}, becomes greater than I_{ref}, the current through R_{ref}, the output

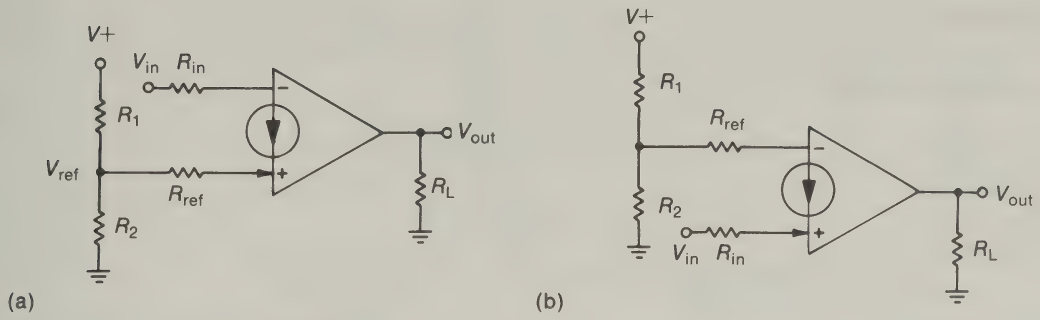


Figure 7-13. The comparator

voltage changes states. As was the case with conventional op amp comparators, the Norton comparator operates at the upper and lower limits of the amp's output and ground ($V+ - 1V$ and V_{BE}). Note that $V+ - 1V = V_{sat}$, and V_{BE} is as close to ground as possible.

The output of the inverting amplifier will be held at V_{sat} as long as V_{ref} is greater than V_{in}. If V_{in} becomes greater than V_{ref}, the output voltage will go to ground potential. The opposite results are obtained with the noninverting configuration. The type of comparator can be diagnosed at a glance, simply by observing where the signal is applied. As an example, the noninverting comparator has V_{in} applied to the noninverting input.

Topic Review 7-7

1. In a typical Norton comparator, the ______ ______ is established by a resistive voltage divider.

2. In the resistive voltage divider, $R_1 + R_2$ should equal ______ to ______ the value of the input resistor.

3. The value of V_{ref} must be greater than ______, or V_{BE}.

4. In an inverting Norton comparator, if I_{in} is greater than I_{ref}, the output will go to ______, which is as close to ground potential as possible.

5. Notice that ______ actually equals $V+ - 1V$, and that ______ is as close to ground as possible. These are the two possible output states with the Norton comparator.

Answers:

1. reference voltage
2. $\frac{1}{10}, \frac{1}{100}$
3. +0.6 VDC
4. V_{BE}
5. V_{sat}, V_{BE}

7-8 Schmitt Triggers

Schmitt triggers are simply comparators with hysteresis. This means that the comparator output changes state at a different value of input voltage for a positive going signal, **(upper trip point, utp)**, than for a negative going signal, **(lower trip point, ltp)**. Hysteresis is provided by regenerative feedback from the output to the noninverting input. This makes the Schmitt trigger an excellent noise and transient eliminator, since voltages between the upper and lower trip points cause no change in output. The Schmitt trigger may be constructed in either inverting or noninverting form, as shown in **Figures 7-14a** and **7-14b**. Unlike the simple comparators, where the input resistors are made equal and a desired value of reference voltage is applied, the Schmitt trigger usually uses $V+$ as the reference voltage, and appropriate values of input resistors are calculated to accommodate the desired upper and lower trip points.

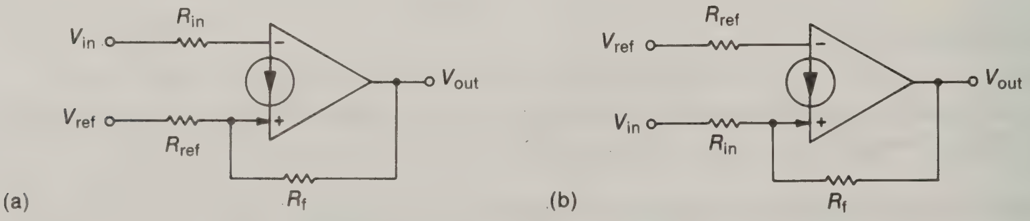


Figure 7-14. The Schmitt trigger

Referring to **Figure 7-15**, reference current is supplied to the inverting input according to the value of $V+$ and resistor R_{ref}. As voltage V_{in} increases, so must current I_{in}, until it exceeds the current flowing from the inverting input (I_{ref}). At this point, the output swings from low to high. This voltage level is the upper trip point (utp). When the output swings high, current flows through the feedback resistor (R_f), from the noninverting input to the output.

When the value of V_{in} decreases, it must decrease until the value of currents I_{in} and I_f drop below the level of reference current (I_{ref}). The output can then swing low.

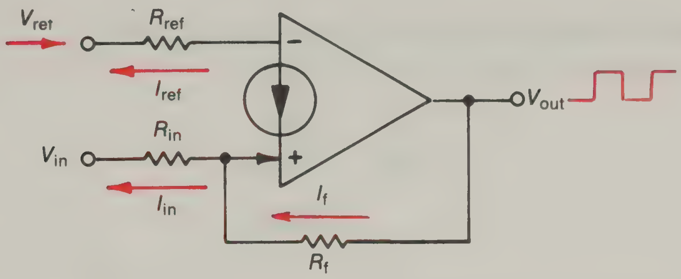


Figure 7-15. Noninverting Schmitt trigger with feedback

This is the lower trip point (ltp).

Notice that if I_f is greater than I_{ref}, the output will never be able to return to the low state. The value of resistor R_f must be made large enough to prevent this condition.

The upper trip point (utp) occurs when:

$$I_{ref} = I_{in} \tag{7-38}$$

so we can say:

$$\frac{V+}{R_{ref}} = \frac{V_{in}}{R_{in}} \tag{7-39}$$

therefore:

$$V_{in} = \frac{V+(R_{in})}{R_{ref}} \tag{7-40}$$

or:

$$\text{utp} = \frac{V+(R_{in})}{R_{ref}} \tag{7-41}$$

The lower trip point (ltp) occurs when:

$$I_{ref} = I_{in} + I_f \tag{7-42}$$

$$\frac{V+}{R_{ref}} = \frac{V_{in}}{R_{in}} + \frac{V+ - 1\ V}{R_f} \tag{7-43}$$

$$\frac{V+C}{R_{ref}} - \frac{V+ - 1\ V}{R_f} = \frac{V_{in}}{R_{in}} \tag{7-44}$$

$$\left(\frac{V+}{R_{ref}} - \frac{V+ - 1\ V}{R_f}\right) R_{in} = V_{in} \tag{7-45}$$

$$\left(\frac{V+}{R_{ref}} - \frac{V+ - 1\ V}{R_f}\right) R_{in} = \text{ltp} \tag{7-46}$$

To design a noninverting Schmitt trigger, choose a value of R_{ref} and calculate the values of R_{in} and R_f. This will provide the desired trip points.

By rearranging equation (7-39):

$$\frac{V+}{R_{ref}} = \frac{\text{utp}}{R_{in}} \qquad (7\text{-}47)$$

$$R_{in} = \frac{\text{utp}(R_{ref})}{V+} \qquad (7\text{-}48)$$

And by rearranging equation (7-43):

$$\frac{V+}{R_{ref}} = \frac{V_{in}}{R_{in}} + \frac{V+ - 1\ V}{R_f} \qquad (7\text{-}49)$$

$$\frac{V+}{R_{ref}} - \frac{V_{in}}{R_{in}} = \frac{V+ - 1\ V}{R_f} \qquad (7\text{-}50)$$

$$\frac{V+ - 1\ V}{\dfrac{V+}{R_{ref}} = \dfrac{\text{ltp}}{R_{in}}} = R_f \qquad (7\text{-}51)$$

As a last step, check to see that I_f is less than I_{ref}.

As a example, let's design a noninverting Schmitt trigger with an utp of 8 volts, and an ltp of 4 volts, operating with a 10 volt $V+$.

Choose a value of R_{ref} to limit current to the Norton amplifier.

Given: $R_{ref} = 1\ M\Omega$ (manufacturer's recommended value)

From (7-48):

$$R_{in} = \frac{\text{utp}(R_{ref})}{V+}$$

$$R_{in} = \frac{8\ V(1\ M\Omega)}{10\ V}$$

therefore:

$$R_{in} = 800\ k\Omega$$

then:

$$R_f = \frac{V+ - 1\ V}{\dfrac{V+}{R_{ref}} - \dfrac{\text{ltp}}{R_{in}}}$$

$$R_f = \frac{9\ V}{\dfrac{10\ V}{1\ M\Omega} = \dfrac{4\ V}{800\ k}}$$

$$R_f = \frac{9\ V}{0.00001 - 0.000005}$$

$$R_f = \frac{9\ V}{0.000005}$$

therefore: $$R_f = 1.8\ M\Omega$$

Checking to see that $I_f < I_{ref}$:

$$I_f = \frac{V+ - 1\ V}{R_f}$$

$$I_f = \frac{10 - 1\ V}{1.8\ M\Omega}$$

$$I_f = 5\ \mu A$$

$$I_{ref} = \frac{V+}{R_{ref}}$$

$$I_{ref} = \frac{10\ V}{1\ M\Omega}$$

$$I_{ref} = 10\ \mu A$$

therefore: $I_f < I_{ref}$, since $I_f = 5\ \mu A$ and $I_{ref} = 10 \mu A$.

In the inverting Schmitt trigger shown in **Figure 7-16**, reference current is applied to the noninverting input, causing the output to be high when the signal voltage is low. This causes current to flow through R_f and also to be added to the reference current.

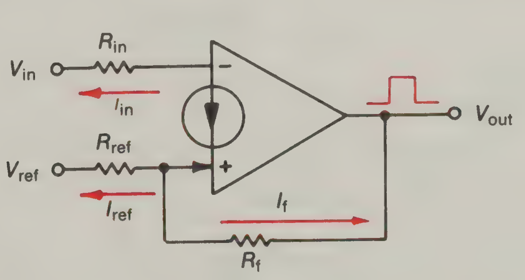


Figure 7-16. Inverting Schmitt trigger with feedback

As the input signal voltage increases, so does the current flowing through R_{in}. The upper trip point (utp) occurs when I_{in} just exceeds $I_{ref} + I_f$. The input signal current must become much larger than the reference current to cause the output to change states.

As the input signal voltage decreases, it must decrease until it is slightly less than the reference current, to cause the output to go high again. This is the lower trip point (ltp).

The lower trip point (ltp) occurs when:

$$I_{\text{in}} = I_{\text{ref}} \tag{7-52}$$

$$\frac{V_{\text{in}}}{R_{\text{in}}} = \frac{V+}{R_{\text{ref}}} \tag{7-53}$$

$$\text{ltp} = V_{\text{in}} = \frac{V+(R_{\text{in}})}{R_{\text{ref}}} \tag{7-54}$$

The upper trip point (utp) occurs when:

$$I_{\text{in}} = I_{\text{ref}} + I_{\text{f}} \tag{7-55}$$

$$\frac{V_{\text{in}}}{R_{\text{in}}} = \frac{V+}{R_{\text{ref}}} + \frac{V+ - 1\ V}{R_{\text{f}}} \tag{7-56}$$

$$\text{utp} = V_{\text{in}} = R_{\text{in}} \left(\frac{V+}{R_{\text{ref}}} + \frac{V+ - 1\ V}{R_{\text{f}}}\right) \tag{7-57}$$

Once again, it should be noted that resistor R_{f} must be sufficiently large enough to limit the feedback current to a value that will allow I_{in} to exceed $I_{\text{ref}} + I_{\text{f}}$, or the output will never be able to go low.

To design an inverting Schmitt trigger, select a value of reference resistor R_{ref}, to limit the current going into the Norton amplifier.

Then, by rearranging equation (7-53):

$$R_{\text{in}} = \frac{\text{ltp}(R_{\text{ref}})}{V+}$$

and by rearranging equation (7-56)

$$\frac{\text{utp}}{R_{\text{in}}} - \frac{V+}{R_{\text{ref}}} = \frac{V+ - 1\ V}{R_{\text{f}}} \tag{7-58}$$

therefore:

$$\frac{V+ - 1\ V}{\dfrac{\text{utp}}{R_{\text{in}}} - \dfrac{R_{\text{f}}}{R_{\text{ref}}}} = V+ \tag{7-59}$$

The last step is to ensure that $I_{\text{f}} + I_{\text{ref}}$ is less than I_{in}.

As an example, let's design an inverting Schmitt trigger having an upper trip point of 10 volts, a lower trip point of 2 volts, and a 12 volt $V+$.

First, choose a value of R_{ref}. Let's use 3 $M\Omega$. This may seem somewhat high, but consider that in the inverting Schmitt trigger, I_{in} must be able to overcome $I_{ref} + I_f$. If the value chosen for R_{ref} is too low, the size of R_{in} may be too small to limit current to the Norton.

$$R_{in} = \frac{\text{ltp}(R_{ref})}{V+}$$

$$R_{in} = \frac{2\ V\,(3\ M\Omega)}{12}$$

$$R_{in} = 500\ k\Omega$$

then: $$R_f = \frac{V+ - 1\ \text{V}}{\dfrac{\text{utp}}{R_{in}} - \dfrac{V+}{R_{ref}}} \tag{7-60}$$

$$R_f = \frac{11}{\dfrac{10}{500\ k} - \dfrac{12}{3\ \Omega}}$$

$$R_f = \frac{11}{0.00002 - 0.000004}$$

$$R_f = \frac{11}{0.000016}$$

$$R_f = 687.5\ k\Omega$$

To be sure that $I_{ref} + I_f < I_{in}$:

$$I_{in} = \frac{\text{utp}}{R_{in}} = \frac{12}{500\ k} = 24\ \mu A$$

$$I_{ref} + I_f = \frac{V+}{R_{ref}} + \frac{V+ - 1\ \text{V}}{R_f} = \frac{12}{3\ M\Omega} + \frac{11}{687.5\ \Omega}$$

$$= 4\ \mu A + 15\ \mu A = 20\ \mu A$$

therefore: $I_{ref} + I_f < I_{in}$, since $20\ \mu A < 24\ \mu A$.

Topic Review 7-8

1. Schmitt triggers are simply ______ that provide regenerative feedback from the

output to the noninverting input.

2. This type of circuit changes state whenever an ______ ______ ______ or a ______ ______ ______ is reached. This makes the Schmitt trigger an excellent noise and transient eliminator, since voltages between the utp and ltp do not cause a change in output.

3. In all cases, ______ must never exceed I_{ref}, or the output will not be able to return to a low state.

4. The upper trip point occurs when ______ is greater than or equal to ______ .

5. The lower trip point occurs when ______ is greater than or equal to ______ .

Answers:

1. comparators
2. upper trip point, lower trip point
3. I_f
4. I_{ref}, I_{sig}
5. I_{ref}, $I_{sig} + I_f$

7-9 Voltage Controlled Oscillators (VCO)

The Voltage Controlled Oscillator (VCO) is essentially a voltage to frequency converter, comprised of an integrator circuit and a noninverting Schmitt trigger, as shown in **Figure 7-17**.

To begin our analysis of the VCO, we will assume some conditions for the circuit of **Figure 7-17.** At time $T = 0$, the output of the integrator is starting to ramp from negative to positive, the output of the Schmitt trigger is low, and transistor Q_1 is cut off. Current to the noninverting input must be twice the value of current to the inverting input of the integrator, because of the designated values of R_1 and R_2.

Capacitor C_1 charges, causing the output of the integrator to charge from negative to positive, until the upper trip point of the Schmitt trigger is reached. When the utp is reached, the output of the Schmitt trigger goes positive, causing transitor Q_1 to saturate.

The noninverting input voltage drops to nearly zero, due to Q_1 being saturated. This causes the output voltage of the integrator to ramp negative as capacitor C_1 discharges.

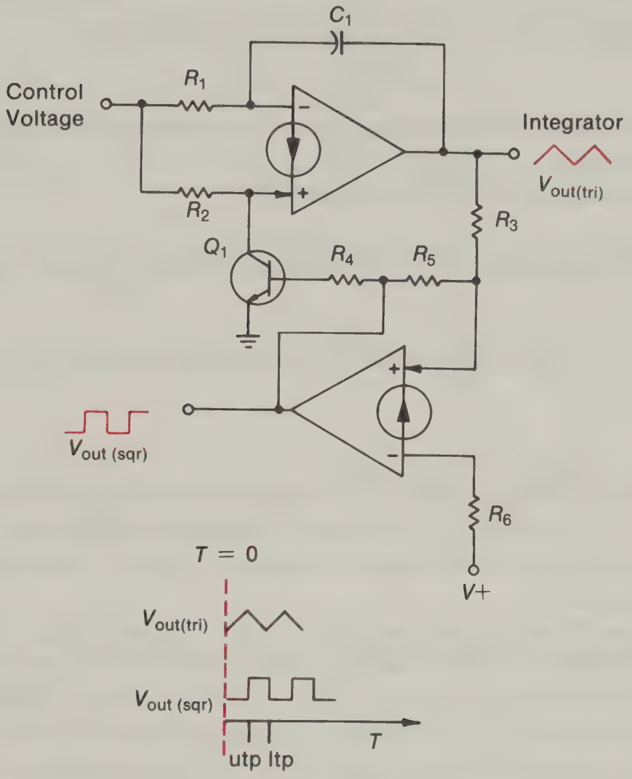


Figure 7-17. A voltage controlled oscillator

The integrator ramps negative until I_{R_6} becomes greater than $I_{R_3} + I_{R_5}$. At this point, the output of the Schmitt trigger goes low, cutting off Q_1. When Q_1 goes low, the current is restored to the noninverting input, causing the output of the integrator to ramp positive once again.

The output frequency of the VCO is controlled by several factors. The control voltage and the R_1C_1 time constant determine how quickly the integrator ramps positive and negative to the upper and lower trip points of the Schmitt trigger. **The output frequency of the Schmitt trigger is then controlled by its upper and lower trip points (utp and ltp), and the value of $V+$ because $V+$ establishes the reference current to the Schmitt trigger.**

Mathematically, the output frequency of the Schmitt trigger is found by:

$$f_{\text{out}} = \frac{I_{R_1}}{2(\text{utp} - \text{ltp})C_1} \tag{7-61}$$

$$\text{where: } I_{R_1} = \frac{V_C - V_{BE}}{R_1} \; (V_{BE} = +0.6 \text{ volts}) \tag{7-62}$$

To design the Schmitt trigger stage, use the procedure for implementing a noninverting Schmitt trigger.

Then, choose a value for R_6 to limit current.

$$R_3 = \frac{\text{utp}}{V+} R_6 \quad \text{(from equation (7-48) of noninverting Schmitt triggers)}$$

$$R_5 = \frac{V+ - 1\ V}{\dfrac{V+}{R_{\text{out}}} - \dfrac{\text{ltp}}{R_3}} \quad \text{(from equation (7-51) of noninverting Schmitt triggers)}$$

The upper and lower trip points should be chosen as close to the supply rails as possible ($V+$ Gnd), to allow for maximum amplitude of the integrator output. The supply rail refers to being as close to (+) or (−) the supply voltage or as close to ground as possible.

Resistor R_4 should be chosen so that a high output from the Schmitt trigger saturates Q_1, but limits the current to the base of the NPN to approximately 3 mA.

For the integrator section of the VCO, choose a value of resistance (R_1) that supplies proper bias current to the Norton amplifier (10 to 200 μA), over the range of the control voltage. Make resistor R_2 half of R_1. Choose a capacitor (C_1) which provides the desired frequency range by rearranging the frequency formula:

$$C_1 = \frac{I_{R_1}}{2(\text{utp} - \text{ltp})\, f_{\text{out}}} \tag{7-63}$$

Where f_{out} is the minimum frequency of operation.

By changing the *RC* time constant of the integrator, the frequency range can be varied as desired. If the *RC* time constant is made longer, the output frequency decreases, and if the *RC* time constant is made shorter, the output frequency increases.

As an example, let's design a VCO to operate from 1 *kHz* to 5 *kHz*, where *V* controls ranges from 2 to 10 volts, with $V+$ equal to 12 volts.

First, pick values for the upper and lower trip points of the Schmitt trigger, close to the supply rails. Since V+ is 12 volts, let's pick the utp to be 11 volts and the ltp to be 1 volt.

Next, pick a value of R_6 to limit current to the Schmitt trigger. Let's say 2 $M\Omega$.

then:

$$R_3 = \frac{\text{utp}}{V+}\,(R_6)$$

$$R_3 = \frac{11}{12}\,(1\ M\Omega)$$

$$R_3 = 910\ k$$

next:

$$R_5 = \frac{V+ \,-\, 1\ V}{\dfrac{V+}{R_6} - \dfrac{\text{ltp}}{R_3}}$$

$$R_5 = \frac{11}{\dfrac{12}{1\ M\Omega} - \dfrac{1}{910\ k}} = \frac{11}{0.000012 \,-\, 0.0000011}$$

$$R_5 = 1\ M\Omega$$

R_4 must be chosen to allow saturation of the NPN, but limit the base current to approximately 3 mA.

therefore: $$R_4 = \frac{V+ \,-\, 1\ V}{3\ mA} = \frac{11\ V}{3\ mA} = 3.7\ k\Omega$$

Calculate the value of R_1 to provide a minimum 10 μA of current at the minimum control voltage.

first: $$R_1 = \frac{V_{C\min}}{I_{\min}}$$

$R_1 = \dfrac{1\ V}{10\ \mu A}$ $-V_{BE}$ is omitted at this point to pad the current slightly

$$R_1 = 100\ k\Omega$$

then: $$R_2 = \tfrac{1}{2}\,R_1$$

so: $R_2 = 50\ k$ $\qquad I_{2(\max)} = 100\ \mu A$

next, the value of C_1 is calculated from the rearranged frequency formula:

$$C_1 = \frac{I_{R1\ (\min)}}{2\,(\text{utp} \,-\, \text{ltp})\,f_{\text{out}(\min)}}$$

$$C_1 = \frac{10\ \mu A}{2\,(11 - 1)\,(1000)}$$

$$C_1 = \frac{10\ \mu A}{20{,}000}$$

$$C_1 = 500\ pF$$

When the control voltage reaches maximum, the output frequency is also maximum.

when: $$V_C = 10\ V$$

$$I_{R_{1(\max)}} = \frac{V_C - V_{BE}}{R_1} = \frac{10 - 0.05}{100\ k} = 50\,\mu A$$

then: $$f_{\text{out}(\max)} = \frac{50\ \mu A}{2\,(11 - (500\ pF)} = \frac{50\ \mu A}{20\,(500\ pF)}$$

$$= \frac{50\ \mu A}{0.01\ \mu A}$$

finally: $$f_{\text{out}(\max)} = 5\ kHz$$

Generally, this design procedure produces only an approximation of the desired output frequency range. This is due largely to the non-linear effect of V_{BE} on the integrator's input current, over the range of V_C. Obviously, V_{BE} has a greater impact at the lower end of the V_C range, where it may be half the value of the control voltage, than it does at the upper end of the range, where V_{BE} becomes only a small fraction of the control voltage. This relationship also makes it somewhat difficult to scale the VCO's output frequency range.

An alternative method of designing the Norton VCO is to design for center frequency, using the same design procedure. Using this method, the Schmitt trigger is designed in the same manner as before, but the integrator is designed to accept the median control voltage

$$V_C(\text{med}) = V_C(\text{min}) - \left(\frac{V_C(\text{max}) - V_C(\text{min})}{2}\right)$$

and therefore, medium input current ($I_{R_1} = 55\ \mu A$ for the design example above) and produce the VCO's center frequency.

In any event, the output frequency range of either design can be modified in three ways. The frequency range can be shifted upward by decreasing the value of the input resistance pair or the feedback capacitor of the integrator or by bringing the upper and lower trip points of the Schmitt trigger closer together. As a last resort, the input control voltage range may be modified to produce the desired output frequency range.

7-10 Summary Points

1. Norton amplifiers are current differencing amplifiers. They are current operated devices.
2. They may be used with input voltages that exceed $V+$, providing input limiting resistors are used.
3. Both inputs will be at +0.6 volts (V_{BE}) under normal operating conditions.
4. Substantial amounts of series input resistance must be used with Norton amplifiers.
5. Norton amplifiers normally operate with a single power supply voltage.
6. The Norton amplifier is normally used as an AC amplifier.
7. Norton amplifiers do not have the extremely high gain (2800) of conventional op amps.
8. A current mirror provides the noninverting inputs ($I+ = I-$).
9. The gain stage is a common emitter amplifier with a constant current source in the collector circuit.
10. For closed-loop applications, the output must be biased to some DC voltage level.
11. Norton amplifiers come in quad (4 per chip) packages.
12. NV_{BE} biasing is used in low noise applications.
13. Common mode biasing is used in DC applications to allow zero and negative voltage levels to be used at the inputs.
14. Norton amplifier comparator outputs operate at zero volts and $V+ - 1$ volt.
15. When $I+$ is greater than $I-$, the output will be $V+ - 1$ volt. When $I- > I+$, the output will be zero volts.

16. Schmitt triggers are comparators with hysteresis. The upper trip point (utp) and lower trip point (ltp) are at different levels. This is accomplished by using regenerative feedback.

17. A voltage controlled oscillator is a voltage to frequency converter.

18. The VCO consists of an integrator, a noninverting Schmitt trigger, and a transistor "switch."

19. Once a VCO is configured, the output frequency is directly proportional to the input voltage.

20. Common mode biasing is achieved by constructing equal resistor networks between V+ and the two inputs. Common mode biasing must be constructed around the type of circuit already in use.

7-11 Chapter Progress Evaluation

1. Draw the schematic symbol of the Norton amplifier, with inverting and noninverting inputs labeled.

2. A linear operating Norton amplifier has a $V+$ of +12VDC. If the amplifier is biased to $\frac{1}{2}$ of $V+$, what does $V_{\text{out(DC)}}$ equal?

3. What is the value of R_b, in the previous example, if R_f equals 20 $k\Omega$?

4. If the voltage out (V_{out}) of a Norton inverting amplifier is 10VDC, and the gain of the amplifier equals 100, what is V_{in}?

5. A Norton inverting amplifier has an input impedance (Z_{in}) of 10 $k\Omega$. If $X_{C\text{in}}$ equals 1 $k\Omega$, what is the value of R_{in}?

6. Using the design parameters for the Norton inverting and noninverting amplifiers, find **(a)** R_f, **(b)** R_b, and **(c)** C_{in}, given the following:

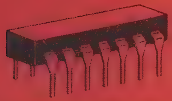
   $Z_{\text{in}} = 10\ k\Omega$
   $A_V = 100$
   $V+ = 12\text{VDC}$
   $V_{\text{out}} = \frac{1}{2}\ V+$

7. Using NV_{BE} biasing, find $V_{\text{out(DC)}}$ if $R_f = 10\ k\Omega$ and $R_b = 1\ k\Omega$.

8. If a noninverting Schmitt trigger has a utp of 10 volts, an ltp of 2 volts, operates from 12 volts $V+$, and has a reference resistance equal to 1 $M\Omega$, find (**a**) R_{in}, and (**b**) R_f.

9. If an inverting Schmitt trigger has a utp of 10 volts, an ltp of 4 volts and a $V+$ of 12 VDC, find (**a**) R_{in}, and (**b**) R_f. Use 1 $M\Omega$ as the value of R_{ref}.

10. Using **Figure 7-17** as a schematic diagram, find the range of f_{out}, if V control ranges from 2 to 10 volts and $V+$ equals 12 volts. The utp is 11 volts and the ltp is 1 volt. Also, $R_6 = 2\ M\Omega$.



Chapter 8

IC Timers

Objectives

Upon completion of this chapter, you should be able to do the following:

- Define what a timer is and explain timer characteristics
- Explain the internal operation of the 555 timer and list its applications
- Explain the operation of the 322 precision timer and list its applications
- Explain the operation of the 2240 programmable timer/counter and list its applications

8-1 Introduction

Timers and their applications are no exception in today's technology. What was once a mechanical apparatus or a series of discrete components is now, in most instances, a simple integrated circuit. These devices can be found in timing applications in home appliances, industrial and aerospace equipment, and in any area where sequential operation is utilized.

Among the most widely used IC timers, are the 555 and 556 (dual 555). As was the case with the integrated circuits we have just studied, these timers are inexpensive, use few external components and are extremely reliable. The single 555 timer can operate accurately from microseconds up to several minutes. Theoretically, this timing range can be extended indefinitely by cascading the timer packages. If a single timer is operating at its outermost limit, the amount of error between the actual and calculated time period increases. By cascading, this error factor is reduced.

As shown in **Figure 8-1**, the 555 timer consists basically of two operational amplifier comparators, three equal valve resistors, two transistor switches, a control flip-flop, and an output stage. Each pin on the 555 is used for a particular function as shown in **Table 8-1**.

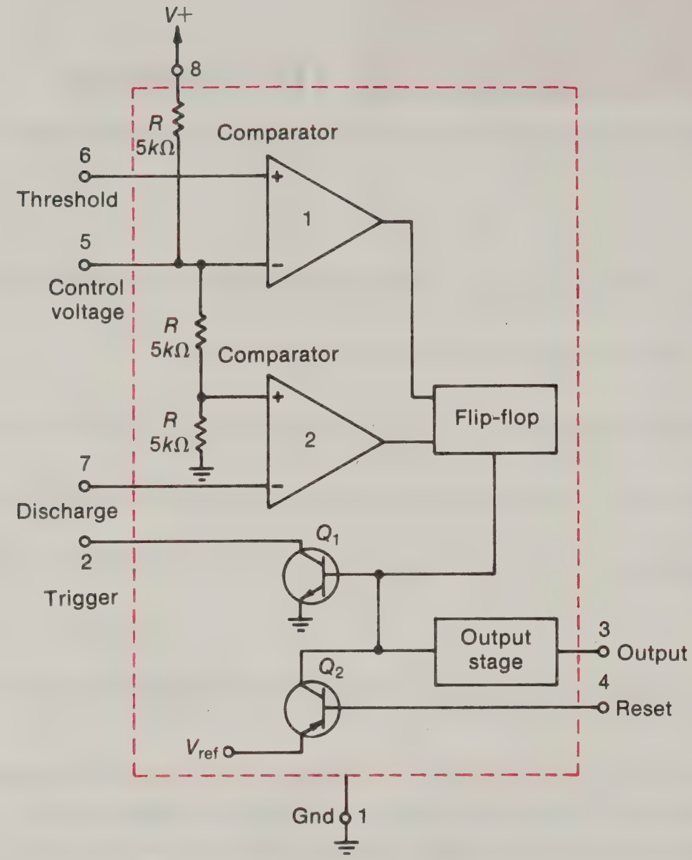

V+
8
R
5kΩ
Comparator
6
Threshold
1
5
Control voltage
R
5kΩ
Comparator
R
5kΩ
2
Flip-flop
7
Discharge
Q_1
2
Trigger
Output stage
3
Output
4
Reset
Q_2
V_{ref}
Gnd 1

Figure 8-1. A 555 integrated circuit timer

Table 8-1. 555 pin function

Pin	Terminology	Function
1	Gnd	Self-explanatory
2	Trigger	Used to start the timing period of the output. The trigger is activated by a low-going pulse.
3	Output	High current type, which will drive TTL logic circuits.
4	Reset	Disables 555. Pin 4 is tied to a logic *high* when not utilized.
5	Control voltage	Used to alter the threshold and trigger operating voltage level. Pin 5 is tied to ground (through a capacitor) when not utilized.
6	Threshold	Used to force the output of the timer *low*. This occurs pin 6 exceeds $\frac{2}{3}$ of *V*+.
7	Discharge	Controls the external timing capacitor.
8	*V*+	Power supply terminal.

The 555 timer comes in two package styles:(A) the TO-99 metal cannister; and (B) the 8 pin mini DIP. The 556 comes in the 14 pin DIP.

The operation of these timers falls into two distinct modes:(1) mono stable, or one shot; and (2) astable, or free running.

Topic Review 8-1

1. A single 555 timer can operate accurately from ______ up to several ______.
2. The 555 timer consists basically of two op amp ______, three equal value resistors, two ______ switches, a control ______-______, and an output stage.
3. The operation of these timers fall into two distinct modes: ______, or one shot; and ______, or free running.

Answers:

1. microseconds, minutes
2. comparators, transistor, flip-flop
3. monostable, astable

8-2 Monostable Timer Operation

The monostable (one shot) timer produces an output pulse of fixed duration, *regardless* of the time length of the input (trigger) pulse. The output pulse duration is determined by the RC time constant established by external components R_t and C_t. The circuit configuration for a monostable timer is shown in **Figure 8-2.**

In the timer's stable state, the output of the comparator is *low* due to the threshold voltage (V_{th}), established by internal resistors R_1 and R_2, on its inverting input. The threshold voltage is always held at 2/3 of $V+$ because the value of R_2 is twice the value of R_1. The output of the control flip-flop is in the set state (output Q is *high*). This positive output is applied to the base of the NPN/transistor (Q_1), causing it to saturate. This shorts out capacitor C_t and puts 0 volts on the noninverting input of the comparator. The output inverter causes the *high* output of the flip-flop to be the *low* output of the timer (Q). Therefore, in the timer's stable state, the output of the monostable timer is low.

When a negative going pulse is applied to the trigger input (pin 2), the output of the flip-flop, Q, goes *low* and the output of the timer, Q, goes *high*. The low output from the control flip-flop cuts off transistor Q_1 and allows capacitor C_t to begin charging up.

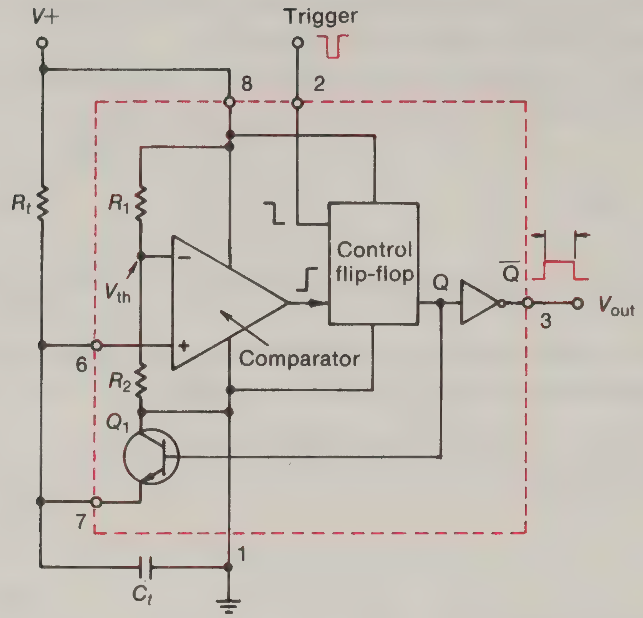


Figure 8-2. A monostable timer

The capacitor charges up, at a rate determined by the *RC* time constant of R_t and C_t, until the voltage across the capacitor slightly exceeds 2/3 of *V*+ (V_{th}). At this point, the output of the comparator goes from *low* to *high*, causing the flip-flop to return to the set state (Q *high*). This returns the entire timer to its stable state.

The timer will remain in its stable state until it is again triggered by a negative going pulse. It should be noted that proper triggering requires the trigger pulse to be shorter than the output pulse.

The duration of the output pulse can be calculated from the formula:

$$P_d = 1.1\, R_t\, C_t \tag{8-1}$$

where P_d = Pulse duration

The capacitor charges to 62.3 percent of *V*+ in one *RC* time constant and the threshold voltage of the comparator is held at 66.6 percent (2/3) of *V*+. Therefore, the capacitor will charge to the threshold voltage in 1.1 time constant and reset the timer output. The internal construction of the timer prevents the value of *V*+ from effecting the output pulse duration. If the value of R_t and C_t is increased, the duration of the output pulse will be increased and conversely, decreasing the value of C_t or R_t will decrease the duration of the output pulse.

Monostable timers are especially useful in batch type industrial applications as opposed to continuous operation. As an example, let's design a timer circuit to control feed water to an industrial holding tank.

The operation of the system is quite simple; when the liquid level in the tank drops to a predetermined level, the feed water control valve should come open for ≈1.7 seconds to refill the tank to its desired level. It is also desirable to have some method to shut-off the feed water, in the event of an over-fill condition.

Start by picking a capacitor and resistor which will give an output pulse of ≈1.7 seconds. Choose C_t first, since there are fewer choices of capacitor values than there are resistor values. Let's choose a 1 μF capacitor.

$$\begin{aligned} \mathrm{P_d} &= 1.1\,(R_t)\,C_t \\ 1.7\ sec &= 1.1\,(R_t)\,1\ \mu F \\ \frac{1.7\ sec}{1.1\,(1\ \mu F)} &= R_t \\ R_t &= 1.5455\ M\Omega \end{aligned}$$

Using a rheostat for R_t will allow us to make the timer variable.The rheostat must be adjustable above the value calculated, in order to allow the output time to be longer or shorter as needed.

Suggested limits of resistor and capacitor values for monostable timers are:

$$\begin{aligned} R_t\ (\mathrm{min}) &= 10\ k\Omega \\ R_t\ (\mathrm{max}) &= 13\ M\Omega \\ C_t\ (\mathrm{min}) &= 100\ pF \\ C_t\ (\mathrm{max}) &= 1000\ \mu F \end{aligned}$$

The minimum pulse duration of the 555 monostable timer is approximately 20 microseconds and the maximum pulse duration is 13,000 seconds, or approximately 3.6 hours.

Topic Review 8-2

1. The monostable timer produces an output pulse of ______ duration, regardless of the ______ ______ of the input (trigger) pulse.
2. The output pulse duration is determined by the ______ time constant established by ______ components.
3. The monostable timer's stable state is ______.
4. The monostable timer will remain in its stable state until it is ______.
5. Proper triggering requires the trigger pulse to be ______ than the output pulse.

Answers:

1. fixed, time length
2. RC_1, external
3. low
4. triggered
5. shorter

8-3 The Astable Timer

As shown in **Figure 8-3,** a 555 configured for astable operation uses both of the timer's internal comparators. This means there will be two threshold voltages established. The upper threshold voltage (V_{uth}) on the inverting input of the upper comparator is held at 2/3 of $V+$ and the lower threshold (V_{lth}) on the noninverting input of the lower comparator is held at 1/3 of $V+$ due to the timer's internal voltage divider (R_1, R_2, and R_3).

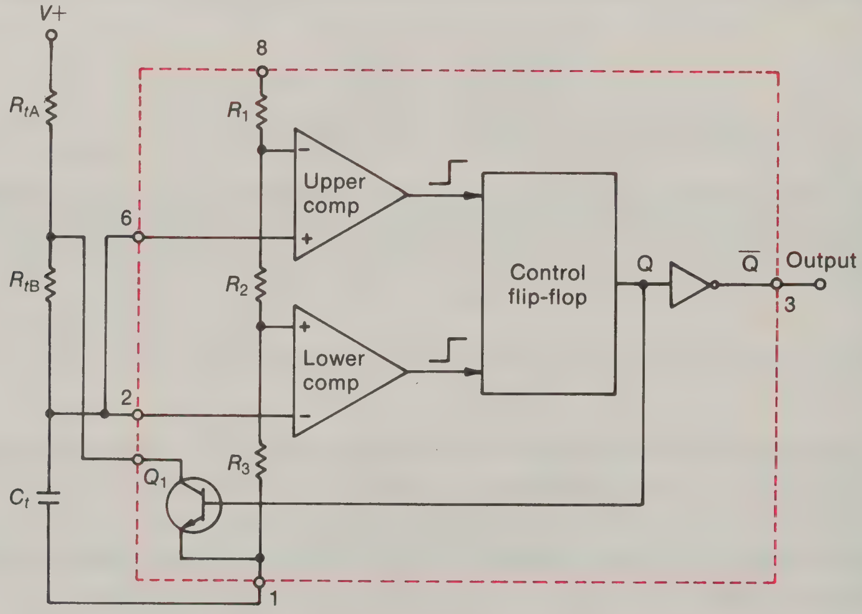


Figure 8-3. The astable timer

Transistor Q_1 allows capacitor C_t to charge and discharge the same as in the monostable timer, but it should be noted that C_t charges through resistors R_{tA} and R_{tB}, but discharges through R_{tB} only.

When power is applied to the circuit, a *low* is applied to the base of Q_1, which allows capacitor C_t to charge through R_{tA} and R_{tB}. C_t will charge until the upper threshold voltage, V_{ut}, is exceeded, causing the upper comparator's output to go *high*. This causes the flip-flop to set (Q to go *high*) and the timer output, Q, to go *low*. The *high* Q output is applied to the base of transistor Q_1 causing it to saturate, which allows capacitor C_t to discharge through R_{tB} and Q_1. At this time, Q_1 acts like a short. The capacitor will discharge until the voltage on the inverting input of the lower comparator drops below the lower threshold voltage, (V_{lth}). This will cause the lower comparator's output to go *high*, bringing the flip-flop output *low*, and the timer output *high*. The low Q output, applied to the base of Q_1, causes the capacitor to begin charging through R_{tA} and R_{tB} again. This order of events will be repeated indefinitely as long as the circuit is not interrupted; this is the *free running* mode.

The astable timer is basically a rectangular wave generator. Since the capacitor charges through R_{tA} and R_{tB} but discharges through R_{tB} only, the time the output is *high* will always be greater than the time the output is *low*.

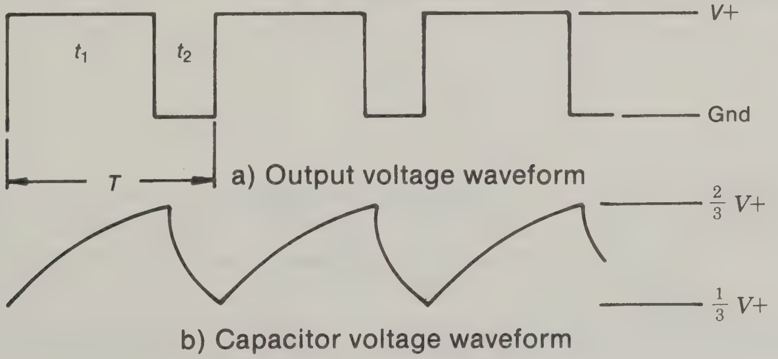


Figure 8-4. Astable output waveforms

As can be seen from Figure 8-4, the ratio of the time that the output is *high* (pulse duration) to one complete cycle of the waveform (pulse period) is known as the duty factor and is normally expressed as:

$$\mathrm{DF} = \frac{t_1}{T} \tag{8-2}$$

The period of the wave is expressed as:

$$T = t_1 + t_2 \tag{8-3}$$

During time 1, (t_1 in Figure 8-4), the capacitor is charging through R_{tA} and R_{tB}. t_1 is expressed by the formula:

$$t_1 = 0.693\,(R_{tA} + R_{tB})\,C_t \tag{8-4}$$

During time 2 (t_2 in Figure 8-4), the capacitor is discharging through R_{t_B} and is expressed as:

$$t_2 = 0.693\ R_{t_B}\ C_t \tag{8-5}$$

Substituting equations 8-4 and 8-5 into equation 8-2, the period of the wave is expressed as:

$$t = 0.693\ (R_{tA} = R_{tB})\ C_t = 0.693\ R_{tB}\ C_t \tag{8-6}$$

Reducing the equation, the period of the wave becomes

$$t = 0.693\ (R_{tA} = R_{tB})\ C_t \tag{8-7}$$

Frequency is the reciprocal of period, so:

$$f = \frac{1}{T} \tag{8-8}$$

$$f = \frac{1}{0.693\ (R_{tA} + 2R_{tB})\ C_t} \tag{8-9}$$

$$f = \frac{1.44}{(R_{tA} + 2R_{tB})\ C_t} \tag{8-10}$$

By substituting equations 8-4 and 8-7 into equation 8-2, duty factor is expressed as:

$$\mathrm{DF} = \frac{0.693\ (R_{tA} + 2R_{tB})\ C_t}{0.693\ (R_{tA} + 2R_{tB})\ C_t} \tag{8-11}$$

therefore:

$$\mathrm{DF} = \frac{(R_{tA} + 2R_{tB})\ C_t}{R_{tA} + 2R_{tB})\ C_t} \times 100\% \tag{8-12}$$

Looking at the 555 astable timer of **Figure 8-5,** if the value of capacitor C_t is increased, the length of t_1 and t_2 will both increase. Therefore, the period (T) of the entire waveform will be increased, which means the frequency of the output wave will be decreased. Conversely, if the value of C_t were decreased, the length of t_1, t_2 and T would all decrease and the output frequency would increase.

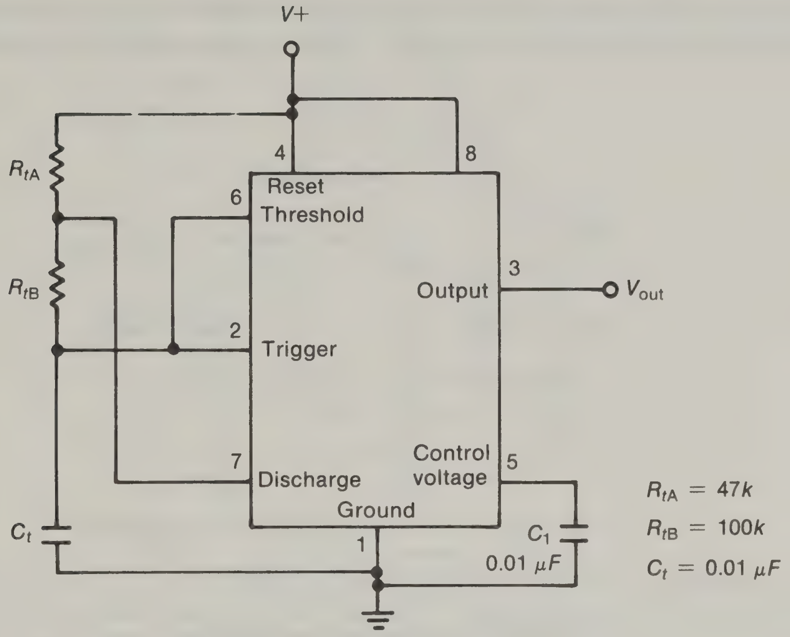

V+
R_{tA}
R_{tB}
C_t
4
8
6
2
7
1
3
5
Reset
Threshold
Output
Trigger
Control voltage
Discharge
Ground
V_{out}
C_1
0.01 μF
R_{tA} = 47k
R_{tB} = 100k
C_t = 0.01 μF

Figure 8-5. A 555 astable timer

If the value of resistor R_{tB} is increased, again both t_1 and t_2 will increase because the capacitor (C_t) charges *and* discharges through R_{tB}. Once again, the period of the wave will be increased and the frequency will decrease. Also, the duty factor will decrease. Decreasing the value of R_{tB} would have the opposite effect.

If the value of resistor R_{tA} is increased, time t_1 will increase, but time t_2 will not since t_2 is determined by the value of C_t and R_{tB} only. The period of the wave will be increased even though t_2 remains constant. Therefore, output frequency will be decreased. Duty factor will be increased because the up-time (t_1) has been increased while the down time (t_2) has been held constant. Decreasing the value of R_{tA} will have the opposite effect.

All of this can be summarized in the following way:

C_t increases: t_1 ↑, t_2 ↑, T ↑ f ↓, DF-

C_t decreases: t_1 ↓, t_2 ↓, T ↓ f ↑, DF-

R_{tB} increases: t_1 ↑, t_2 ↑, T ↑ f ↓, DF↓

R_{tB} decreases: t_1 ↓, t_2 ↓, T ↓ f ↑, DF↑

R_{tA} increases: t_1 ↑, t_2-, T ↑ f ↓, DF↓

R_{tA} decreases: t_1 ↑, t_2-, T ↑ f ↓, DF↓

The astable timer can be configured as in **Figure 8-6** to provide a fifty percent duty factor by placing a diode in parallel with R_{tB} and making R_{tA}, and R_{tB} equal.

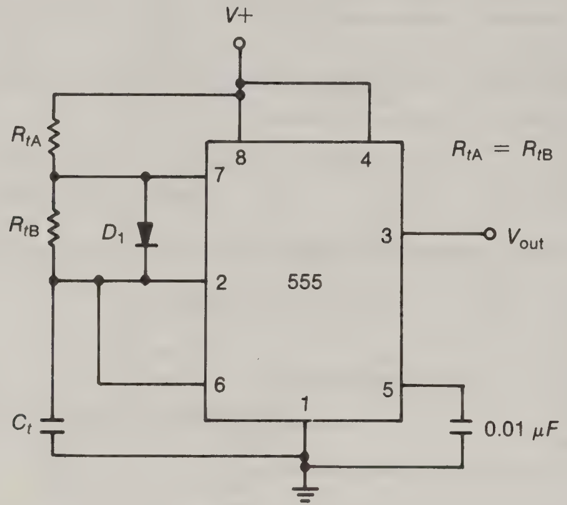


Figure 8-6. Astable timer with 50% duty factor

In this configuration the timing capacitor is charged through R_{tA} only since D_1 is forward biased shunting the charging current around R_{tB}. When the capacitor discharges D_1 becomes reverse biased forcing the discharge current to flow through R_{tB} and the discharge terminal, pin 7. Since R_{tA} equals R_{tB}, the charge and discharge times are equal.

This method of operating the 555 is known as *extended operation.* **The term extended operation applies to any configuration that causes the timer's duty factor to be equal to, or less than 50%.** **Figure 8-7** shows an astable configuration which allows virtually any duty factor to be produced by simply choosing appropriate values of R_{tA}, R_{tB} and C_t.

In this configuration the timing capacitor (C_t) is charged through R_{tA} and D_1 and discharged through R_{tB} and D_2.

The duty factor of this configuration is established by the formula:

$$\mathrm{DF} = \left(\frac{R_1}{R_1 + R_2}\right) \times 100$$

$$R_1 + R_2$$

or:

$$\mathrm{DF} = \left(\frac{R_1}{R_2} + 1\right) \times 100$$

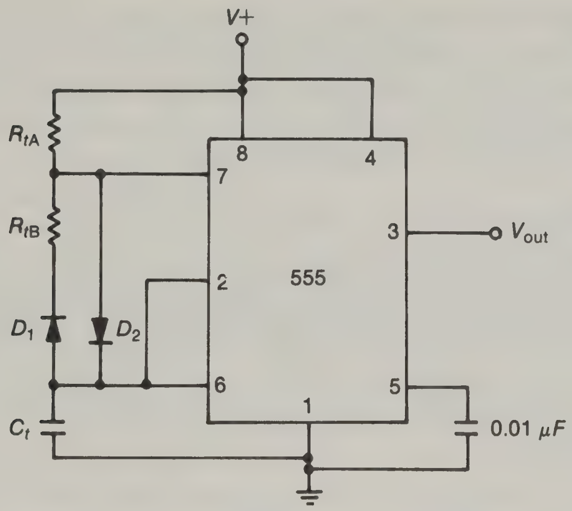


Figure 8-7. Extended duty factor configuration

Do to the presence of the diodes in the extended astable circuits, the timing constant will be increased slightly from the 0.693 value given for the standard astable timer, to a value of approximately 0.75. This constant varies with the value of the supply voltage.

Topic Review 8-3

1. A 555 configured for astable operation uses both of the timer's internal _______.
2. The astable timer is basically a _______ wave generator.
3. The time that the output of the astable timer is _______, will always be greater than the time the output is _______.
4. The ratio of time that the output is high (pulse duration) to one complete cycle of the waveform (pulse period) is known as the _______ _______.
5. The term _______ _______ applies to any configuration that causes the timer's duty factor to be equal to, or less than 50%.

Answers:

1. comparators

2. rectangular
3. high, low
4. duty factor
5. extended operation

8-4 322 Precision Timer

The 322 is a precision timing device which operates in the same manner as the 555 monostable timer. Unlike the 555, astable operation is not available on the chip but the 322 does provide greater flexibility in a number of ways. In addition to the type of internal circuitry found in the 555, the 322 contains: an on board 3.15 volt regulator; a digital-output logic control gate; and a floating output power transistor, as shown in **Figure 8-8.**

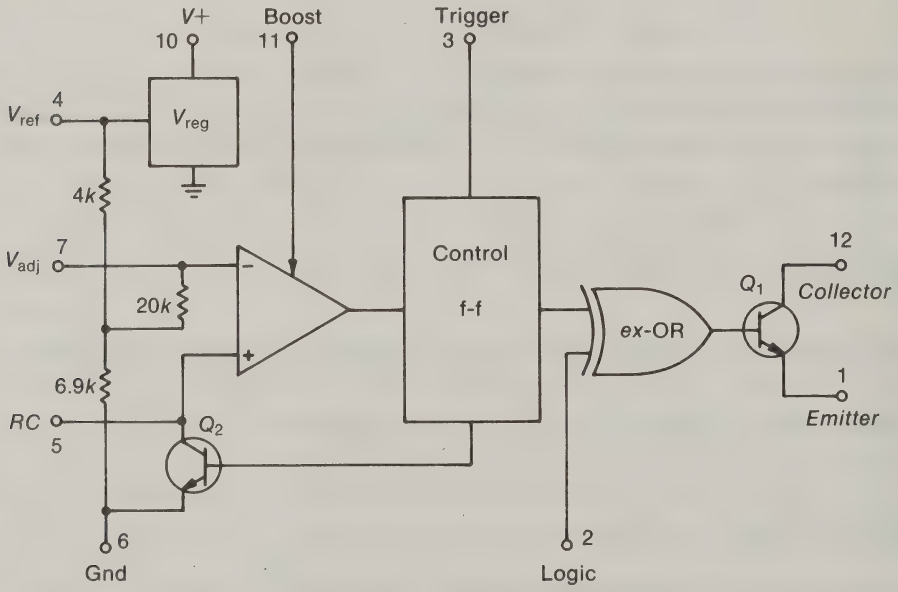


Figure 8-8. A block diagram of the 322 timer

The internal voltage divider produces a threshold voltage (V_{ref}) that is 62.3 percent of the timing voltage (or 1 RC time constant) which allows the duration of the output timing pulse to be calculated by the formula:

$$T = R_t C_t \tag{8-13}$$

The control flip-flop of the 322 controls discharge transistor Q_2 and drives an exclusive-OR logic gate. This allows the user to determine the type of output pulse the timer delivers. The *ex*-OR gate produces a logic *high* output when the voltages on the inputs are at different logic levels. When both inputs are at the same logic level (*high* or *low*, the output of the gate is *low*. One input of the *ex*-OR gate is the chip's logic input pin (pin 2). When the logic pin is held *low*, the output of the *ex*-OR gate will be *high* during the timing pulse and when the logic pin is held *high* the output of the *ex*-OR will be *low* during the timing pulse.

The output of the *ex*-OR gate drives the NPN output power transistor stage (Q_1). Both the **emitter** (pin 1) and collector (pin 12) of the output transistor are available to the user. This allows the output stage to be a common emitter or common collector configuration. The output transistor has internal over-current protection and can drive loads up to 40 volts and 50mA.

The 322 can be used with supplies between 4.5 and 40 volts. The **trigger** input (pin 3), unlike the 555, initiates the timing cycle on a positive going input pulse. The trigger pulse must exceed +1.6 volts and can be as great as +40 volts. In the event that the trigger input is held *high* throughout the timing cycle, the timer will time-out; but the timing capacitor, (externally connected through pin 5), will not discharge and the timer will not retrigger until the trigger input drops below +1.6 volts.

The output of the 3.15 volt internal regulator is available at the **voltage reference pin** (pin 4), and is normally used as the supply for the timing resistor/capacitor voltage divider. The internal reference voltage level is accessible through **voltage adjust**, pin 7. This terminal can be used to externally alter or terminate the timing period. The voltage applied to this terminal should be held below 5 volts. When not in use, this pin should be bypassed to ground with a 0.01 μF capacitor to enhance the chip's noise immunity. The **boost pin** (pin 11) can be used to increase the transition speed of the comparator for use with very short timing pulses, by connecting it to V+.

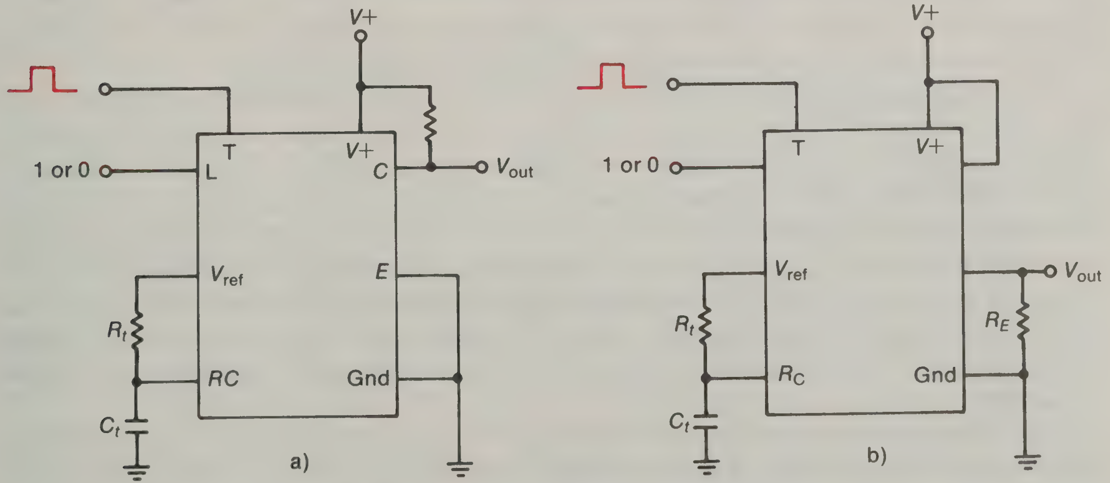


Figure 8-9. Common 322 circuit configurations

Figure 8-9 shows common configurations for the 322 timer with: (a) the output taken from the collector; and (b) with the output taken from the emitter. In part a, the output will be *high* during the timing period if the logic input is held *high*, and *low* during the timing period if the logic input is *low*. In part b of the figure, these relationships will be reversed.

Topic Review 8-4

1. In addition to the 555 type of internal circuitry, the 322 contains: an on board 3.15 volt ______; a digital-output logic ______ ______; and a floating output ______ ______ ______.

2. With the 322, both the ______ and ______ of the output transistor are available to the user.

Answers:

1. regulator, control gate, power transistor
2. emitter, collector

8-5 2240 Programmable Timer/Counter

The 2240 timer/counter is an extremely versatile monolithic IC. It is capable of generating extremely long timing pulses (up to five days) and 255 simultaneous frequencies or 255 distinct pulse patterns from a single *RC* timing network. A block diagram of the 2240 is shown in **Figure 8-10.**

This IC consists of a time base oscillator, or TBO, very similar to an astable 555 timer. An external timing capacitor and resistor set the basic oscillator frequency which is applied to an 8-bit binary counter section. A bit is one piece of binary information, that is a 1 or a 0 expressed as a *high* or *low* voltage level, respectively. Unlike the previous astable timers discussed, the 2240 discharges the timing capacitor directly through the control transistor, making the discharge portion of the output wave form very short. The short discharge time allows the duration of the timing pulse to be thought of as the period (*T*) of the square wave. Due to the relative values of the internal voltage divider, the period of the timing pulse equals one *RC* time constant.

The binary counter section consists of eight toggle type flip-flops. These flip-flops are two stage devices whose outputs change from one logic level to the other (0 to 1 or 1 to 0) when one complete clock pulse is applied to their inputs. On the rising edge of

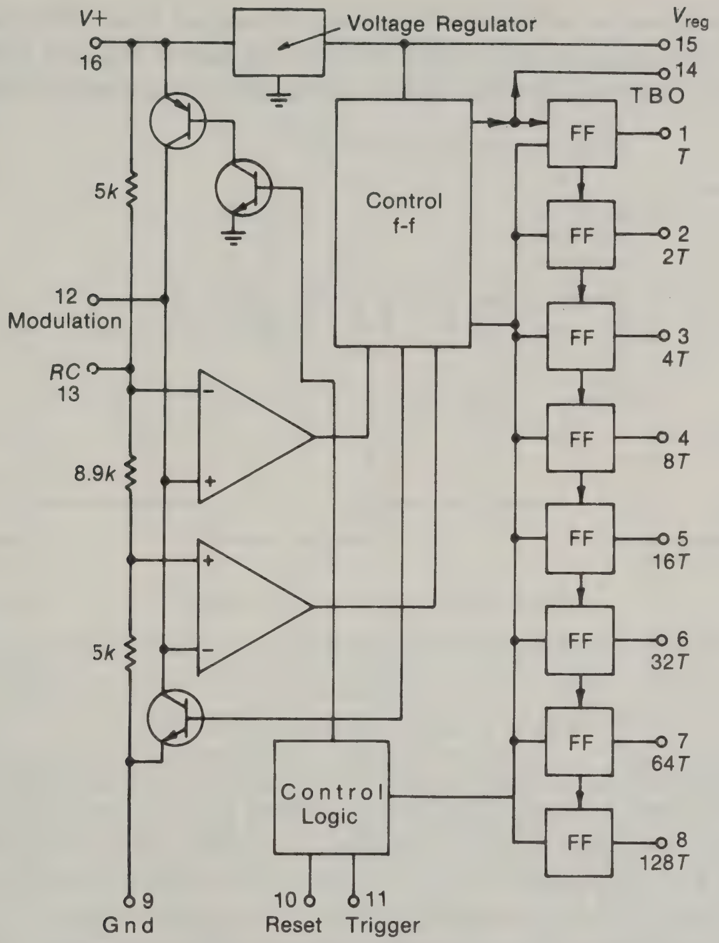

V+
16
Voltage Regulator
V_{reg}
15
14
TBO
Control
f-f
FF
1
T
2
2T
3
4T
4
8T
5
16T
6
32T
7
64T
8
128T
5k
12
Modulation
RC
13
8.9k
5k
Control
Logic
9
Gnd
10
Reset
11
Trigger

Figure 8-10. Block diagram of the 2240 programmable timer /counter

the input pulse, the logic change is loaded into the input stage of the flip-flop. On the falling edge of the input pulse the logic change is transferred to the output. This effectively divides the input frequency by two, since the input pulse must make two logic transitions to create one output transition.

The output of the TBO section, drives the input of the first flip-flop, causing its output to change state each time the TBO generates a complete timing pulse. The output of the first flip-flop, drives the input of the second flip-flop, whose output in turn drives the input of the third, and so on. Each successive flip-flop divides the output frequency of the previous one by two, which is the same as multiplying the original TBO timing pulse by successive powers of two. In other words, the TBO would have to create four complete timing pulses, in order to create a single logic level change, at the output of the third flip-flop (4*t* output). The TBO would then have to make 128 timing cycles to cause the output of the eighth flip-flop (128 *t*) to change states. **Figure 8-11** shows the timing cycle of the 2240 programmable timer/counter.

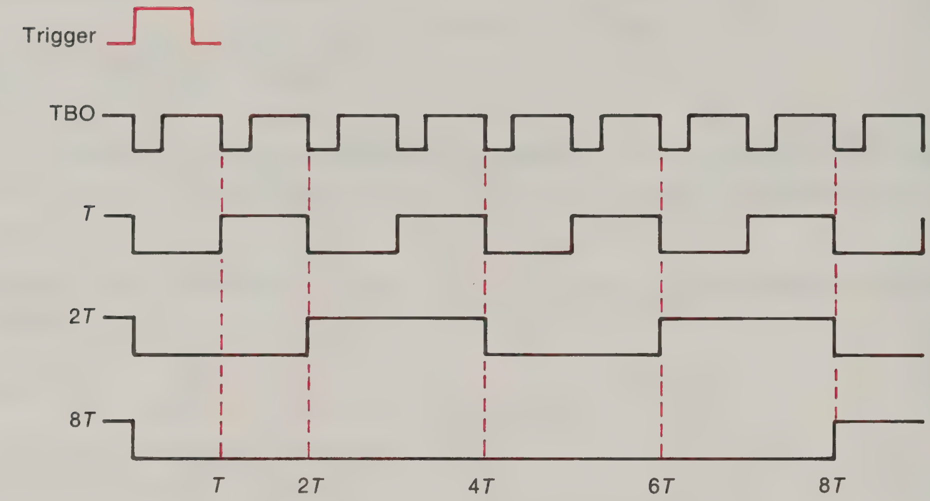


Figure 8-11. 2240 output timing pulses

The 2240 chip also contains an onboard voltage regulator, and internal control circuitry which is used to trigger the TBO and reset the counter section. The outputs of the time base oscillator and the onboard regulator are available to the user through pins 14 and 15, respectively. The value of the regulated output varies slightly with supply voltage. Pin 12 (modulation) provides external access to the upper comparator reference voltage. This allows the user to modify the TBO output period by applying a DC voltage to terminal 12.

The 2240 can be configured to perform either monostable or astable operations. Although the operation of the TBO section is astable in nature, the overall operation of the chip is that of a triggered monostable. The counter output(s) in use are usually tied to the reset terminal. This terminates the TBO operations, and resets the counter section to zero at the end of the timing cycle. The output devices of the timer section are open collector NPN transistors. These may be tied together in a common output line to produce the sum of two or more output time periods. As an example, by tying together output *T* and 2*T*, a timing period of 3*t* would be created.

Figure 8-12 shows a 2240 configured for monostable operation where the duration of the output timing pulse is equal to:

$$P_d = R_t R_t (N) \tag{8-14}$$

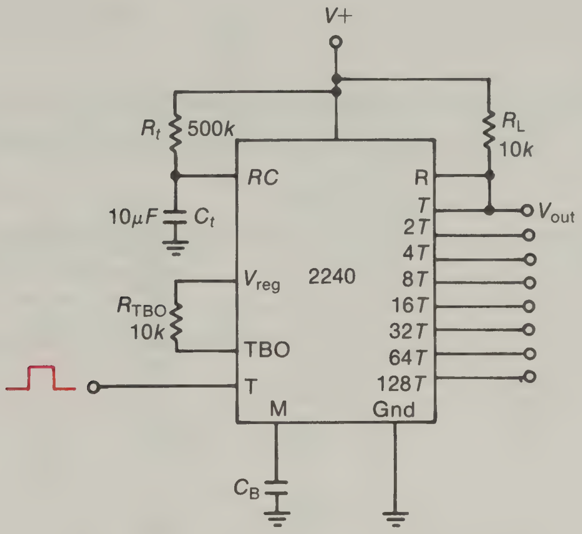


Figure 8-12. 2240 monstable operation

Where N is equal to the sum of the timing cycle outputs tied to V_{out}. When power is first applied to the circuit shown in **Figure 8-12**, the control logic circuitry inhibits the operation of the TBO section by clamping the RC terminal near $V+$ and resets all the counter outputs to the zero state (in their inactive state the counter's outputs are *high*). The application of a positive going trigger pulse initiates the operation of the time base oscillator and causes the counter outputs to go low. The TBO will cycle in the astable mode until enough timing pulses have been created to cause the $8T$ output to change states. When the $8T$ output returns to the high state, a high is applied to the reset input which once again inhibits the TBO operation and returns all of the counter outputs to the high state. After an initial trigger pulse is applied, the chip will not be affected by further triggering until shortly after the application of a reset pulse.

The 2240 accepts a wide range of timing components; the value of R_t should be between 1 $k\Omega$ and 10 $m\Omega$ and C_t should be between 0.01 μF and 1000 μF. R_L serves as the pull-up resistor for the open collector outputs of the counter section. Its value is not critical but should be chosen to limit the output current to below 4 mA. R_{TBO} is a pull-up resistor for the TBO output and is connected to the internal regulator's output. Its value should be in the 20 $k\Omega$ range. C_b is a 0.01 μF bypass capacitor to improve the circuit's noise immunity.

The 2240 astable configuration shown in **Figure 8-13** is very similar to the monostable circuit we just studied. For astable operation, the output is not connected to the reset terminal to automatically terminate the TBO operation at the end of the

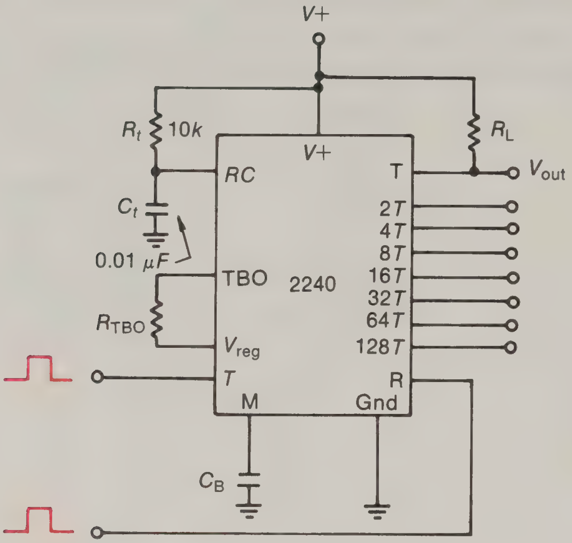

V+
R_t
10k
R_L
V+
RC
T
V_{out}
C_t
2T
4T
8T
0.01 μF
TBO
2240
16T
32T
64T
128T
R_{TBO}
V_{reg}
T
R
M
Gnd
C_B

Figure 8-13. 2240 astable operation

timing pulse. The circuit shown in **Figure 8-12** is not self starting; a trigger pulse must be applied to initiate the astable operation. If a self-starting circuit is desired, the trigger input can be connected to $V+$ or the regulator output.

Once again, the duration of the timing pulse can be calculated by:

$$\mathrm{P_d} = R_t C_t \,\mathrm{N}$$

Since the period (T) of the output consists of two pulse durations:

$$T = 2\, R_t C_t \,\mathrm{N} \tag{8-15}$$

and therefore, the output frequency is:

$$f_{\mathrm{out}} = \frac{1}{2\, R_t C_t \,\mathrm{N}} \tag{8-16}$$

In the case of **Figure 8-13**

$$\mathrm{P_d} = 10k\,(0.1\ \mu F)\,(16) = 0.016\ sec$$

$$T = 2\,(.016) = 0.032\ sec$$

$$f_{\mathrm{out}} = \frac{1}{0.032} = 31.25\ Hz$$

Topic Review 8-5

1. The 2240 timer/counter is capable of generating extremely long _______ _______ and 255 simultaneous frequencies or 255 distinct _______ _______ from a single *RC* timing network.

2. A bit is one piece of binary information, that is, a 1 or a 0 expressed as a _______ or _______ voltage level, respectively.

3. The 2240 can be configured to perform either _______ or _______ operations.

Answers:

1. timing pulses,
   pulse patterns
2. *high,*
   low
3. monostable,
   astable

8-6 Timer Applications

IC timers can be used to perform many functions besides timing and clock pulse generation. **Figure 8-14** shows a 555 timer configured to perform as a Schmitt trigger.

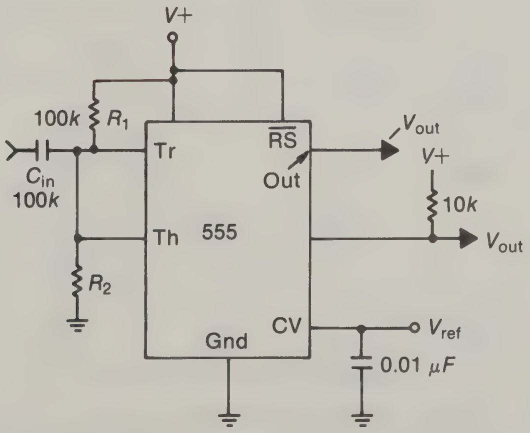

V+
100k
R_1
C_{in}
100k
Tr
$\overline{RS}$
Out
Th
555
R_2
Gnd
CV
V_{out}
V+
10k
V_{out}
V_{ref}
0.01 μF

Figure 8-14. 555 Schmitt trigger

No *RC* timing network is used for this configuration. The input signal is applied to the inputs of both comparators through an input capacitor. The comparators simply compare the input voltage level to the timer's $\frac{2}{3}$ and $\frac{1}{3}$ $V+$ threshold levels, to drive the control flip-flop to its set or reset state. Two outputs are available for this circuit: the normal output on pin 3; and the open collector of the discharge capacitor (pin 7), using a pull-up resistor.

The internal threshold levels can be adjusted by applying a DC voltage (V_{ref}) to pin 5 (control voltage). If this input is used, the upper trip point (utp) of the Schmitt trigger will be equal to V_{ref}, and the ltp will be equal to $\frac{1}{2}$ V_{ref}. The input may be biased to any predetermined level by a resistive voltage divider (R_1 and R_2). In **Figure 8-14** the input is biased to $\frac{1}{2}$ $V+$, meaning the input signal will only have to vary by $\pm\frac{1}{6}$ $V+$ to trip the comparator outputs. The use of input offset is optional. The input capacitor (C_{in}) removes any DC component from the input signal. Its value should be chosen so that $X_{C_{\text{in}}}$ is approximately equal to zero at the circuit's designed frequency of operation.

This circuit can be used to convert an analog frequency signal to a digital frequency, or to restore a noisy or deteriorated digital signal to a clean stable waveform.

The 555 timer is often used as the driving device for LED indicators and inductive loads, such as relays and speakers. **Figure 8-15** shows common methods of configuring the 555's output to drive LEDs.

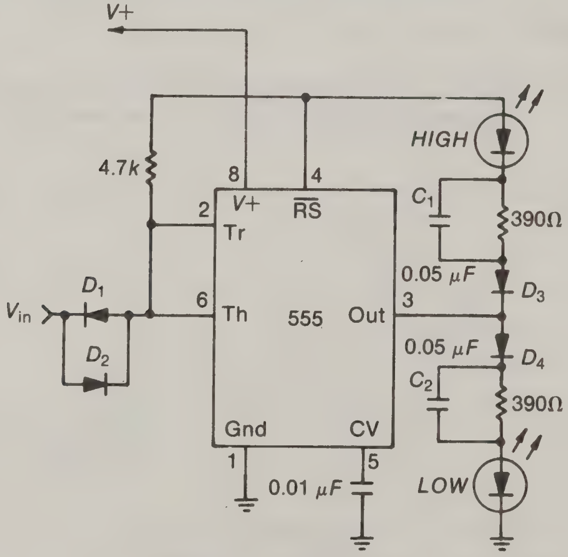


Figure 8-15. 555 LED driver

The output of the 555 must be low to forward bias the upper LED and high to forward bias the lower LED. Resistors must be used to current limit and protect the

LEDs. Values between 200 ohms and 500 ohms are suitable for this purpose.

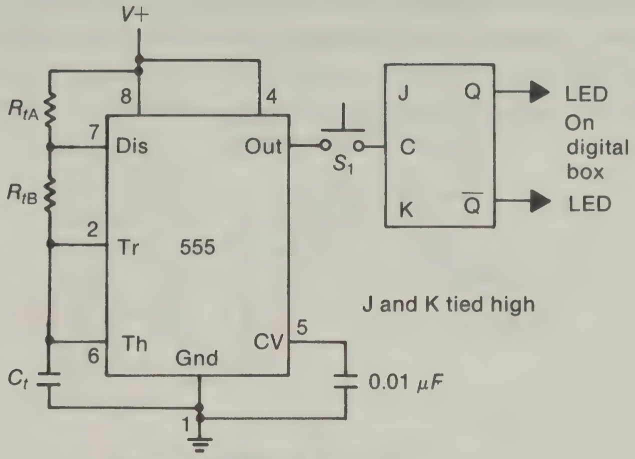

V+
8
4
R_{tA}
7
Dis
Out
S_1
J
Q
C
K
$\overline{Q}$
LED
On digital box
LED
R_{tB}
2
Tr
555
J and K tied high
6
Th
Gnd
CV
5
C_t
0.01 μF
1

Figure 8-16. 555 decision maker

A simple circuit used to make *yes* and *no* decisions is shown in **Figure 8-16**. The output of an astable 555 timer is applied to a toggle type flip-flop through a momemtary contact switch. The operation of the toggle flip-flop has been discussed earlier in this chapter; it can be implemented with a J-K type flip-flop by tying the J and K inputs high, and applying the input signal to the clock (C).

When the switch is depressed, the rectangle-wave output drives the input of the flip-flop causing *high* state to alternate between Q and $\overline{Q}$ ($\overline{Q}$ is not Q). When the switch is released, the flip-flop will latch into one of the two output states.

Figure 8-17 shows common 555 output configurations for driving relay coils. In part a of the figure, the relay will be energized when the output of the timer goes *low*. Diode D_1 clamps the reverse voltage of the relay to protect the IC from high voltages due to inductive kick-back. In part b of the figure, the relay will be energized when the output goes *high*. Diode D_2 is added to prevent reverse voltage spikes across the relay.

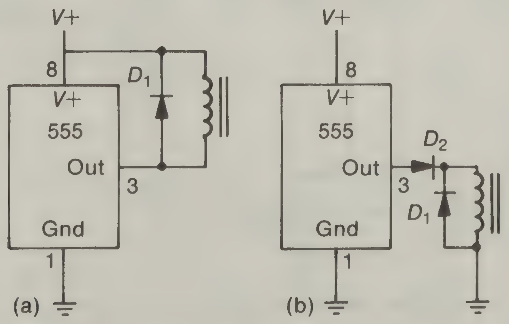

V+
8
V+
555
Out
3
Gnd
1
D_1
(a)
V+
8
V+
555
Out
3
Gnd
1
D_2
D_1
(b)

Figure 8-17. 555 output configurations for driving relays

Figure 8-18 shows a 555 used as the control circuit for a dusk-to-dawn light. This circuit uses a photo resistance element, CDS, and the 555's reset terminal to sense the presence of light. These control a normally open relay contact, which in turn controls the light.

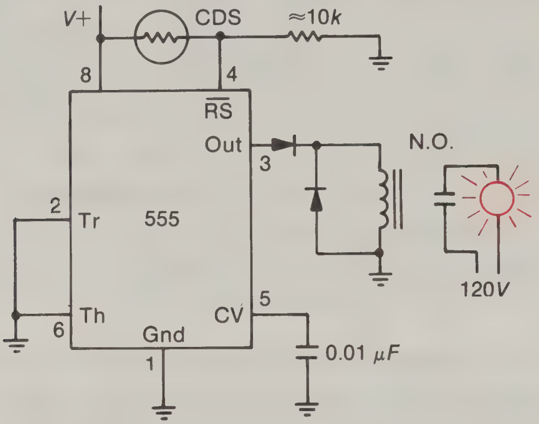

V+
CDS
≈10k
8
4
RS
Out
3
N.O.
2
Tr
555
Th
6
Gnd
1
CV
5
0.01 μF
120V

Figure 8-18. Automatic porch light

In the presence of light, the resistance of the photo-resistor is *high*. This holds the timer's reset terminal and output in the *low* state. When the light source is removed, the resistance of the photo-resistor decreases, and the reset input goes *high*. The timer's output also goes *high*, energizing the relay and closing the contact, thereby causing the light to come on.

A 555 astable timer can also be used to convert DC to an AC signal as shown in **Figure 8-19**.

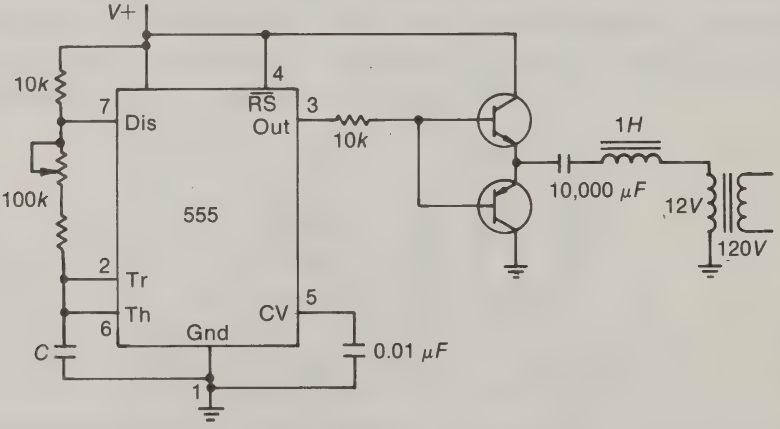

V+
10k
7
Dis
4
RS
Out
3
10k
1H
10,000 μF
12V
120V
100k
555
2
Tr
Th
6
C
Gnd
1
CV
5
0.01 μF

Figure 8-19. 555 DC to AC inverter

The astable timer output is applied to a complementary/symmetry output-current driver stage. The key to the circuit is the bandpass filter comprised of C_1 and L_1. This filter section changes the square wave output of the timer to a sine wave. Finally, the sine wave is applied to a 10:1 step up transformer.

Often a speaker is used as an audible indicator so that visual contact is not necessary to determine the state of a device or process. **Figure 8-20** shows a 555 audible continuity tester.

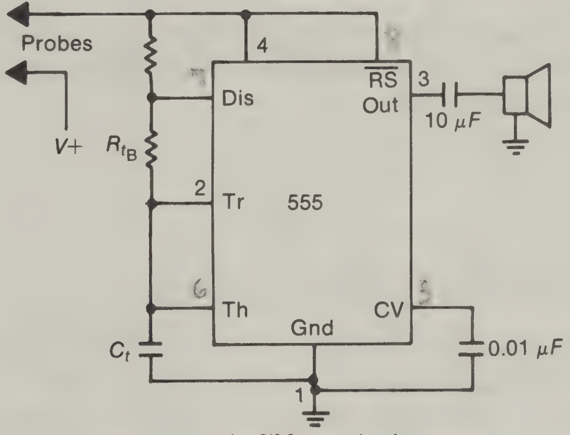

Probes
4
8
7
Dis
RS
Out
3
10 μF
V+
R_{t_B}
2
Tr
555
6
Th
5
CV
Gnd
C_t
0.01 μF
1

Figure 8-20. Audible continuity tester

If continuity is present between the probes, V+ will be applied to the astable 555 circuit causing it to produce an output. The output frequency of the timer will drive the speaker causing it to produce an audible tone. Obviously, if continuity is not present, no tone can be produced by the circuit.

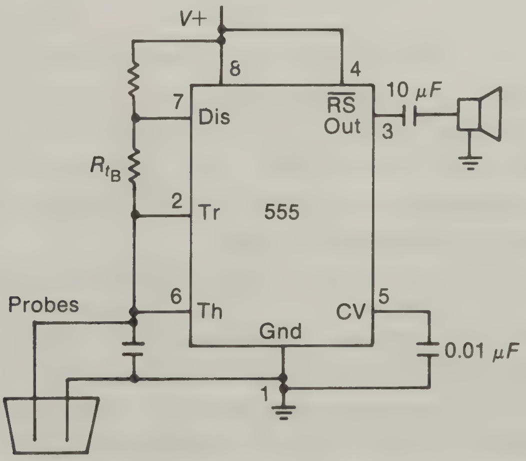

V+
8
4
10 μF
7
Dis
RS
Out
3
R_{t_B}
2
Tr
555
Probes
6
Th
5
CV
Gnd
0.01 μF
1

Figure 8-21. Liquid level detector

Similarily, the astable 555 can be combined with a speaker to detect liquid level as shown in **Figure 8-21**. (Most liquids are electrical conductors. When the probes come into contact with a liquid, they place a short across the timing capacitor which prevents it from charging. Therefore, no tone is produced. If the liquid level drops away from the probes, the short across the capacitor is removed and astable operation takes place. The speaker will produce a tone which corresponds to the frequency of the astable timer).

A similar concept using the 555 is the electronic, variable speed metronome shown in **Figure 8-22**. A metronome is an instrument used by musicians to keep time by a repetitive ticking sound.

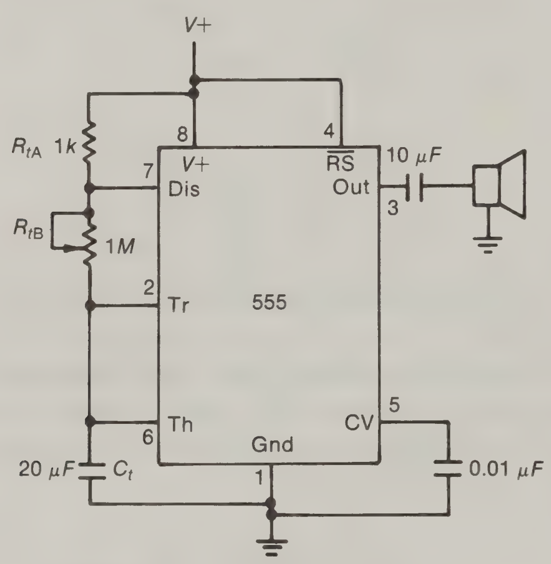


Figure 8-22. Variable speed metronome

Large values of timing components are used with the astable timer to produce long output timing pulses. At the output, the capacitor charges up to block the DC portion of the timing pulse. The classic tick-tock sound is produced because the capacitor allows the speaker to respond only to the change of the timer's output level. The beat can be changed by adjusting R_{TB}.

IC timers are used in a number of other non-timing applications. **Figure 8-23** shows an astable 555 configured as a VCO. In this configuration a DC voltage is applied to the control voltage input (pin 5) to modify the timing period of the astable timer. The minimum frequency of the VCO is established by the frequency of the basic astable operation. When using the control voltage terminal, the applied voltage range should be between 2 volts and (V+) minus one volt. As the control voltage increases from its minimum value, the output frequency decreases at a linear rate.

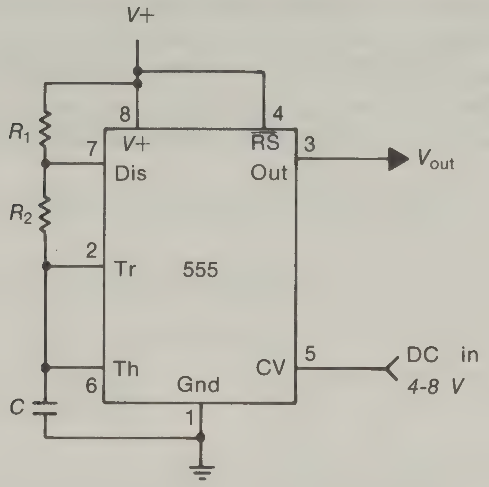

V+
8
4
R1
7
V+
Dis
RS
Out
3
Vout
R2
2
Tr
555
Th
6
Gnd
CV
5
DC in
4-8 V
C
1

Figure 8-23. Astable 555 configured as a VCO

Figure 8-24 shows a 322 timer used to detect digital signals with pulse widths longer than a pre-determined length. With no logic pulse applied to the circuit, transistor switch Q_1 is cut off, holding the logic input (pin T) *low*. When a logic pulse is applied to the input the timer will be triggered by Q_1 which will also be turned on. This pulls the logic input level high and prevents the output from changing states for the duration of the R_tC_t time constant. If the duration of the digital input pulse is longer than one *RC* time constant, the circuit will produce an output pulse whose duration is equal to the duration of the input pulse minus the *RC* time constant.

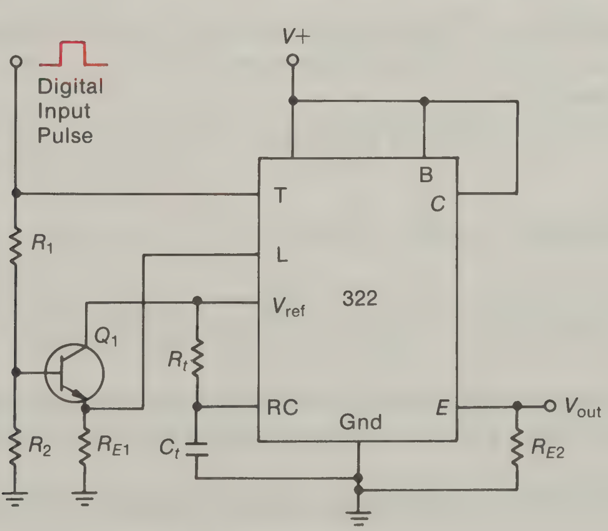

V+
Digital
Input
Pulse
T
B
C
R1
L
Vref
322
Q1
Rt
RC
Gnd
E
Vout
R2
RE1
Ct
RE2

Figure 8-24. 322 pulse width detector

A standard 322 timer configuration can be adapted to provide accurate frequency-to-voltage conversion as shown in **Figure 8-25**. The digital input frequency signal is applied to the trigger input of the 322, and the output is applied to a simple low-pass filter/integrator. The fitler will integrate the output pulse to produce a DC output voltage that is proportional to the pulse width of the output pulses.

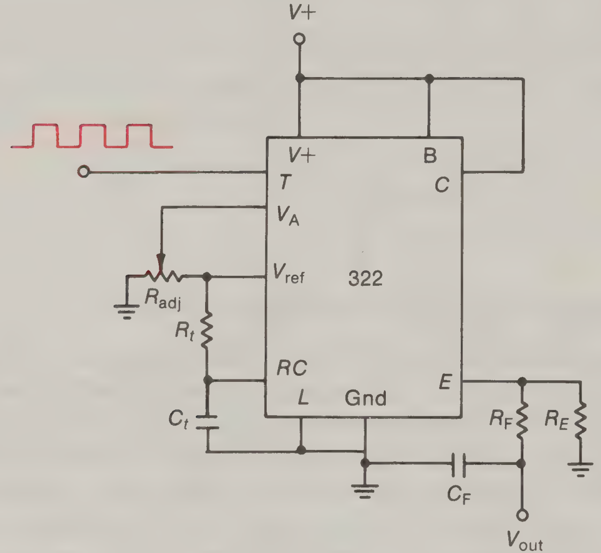


Figure 8-25. 322 frequency to voltage converter

Variable resistor R_{adj} is used to calibrate V_{out} at a given input frequency. The output voltage is an average value determined by the duty factor of the output pulses and can be calculated by:

$$V_{out} = R_t C_t (V+) f_{in} \quad (8\text{-}17)$$

8-7 Summary Points

1. The 555 timer can be used in two different modes: monostable (one shot) and astable (free running).
2. The 555 consists of 3 equal value resistors, two op amp comparators, a control flip-flop, a transistor switch, and an output stage (inverter).
3. The output of the monostable timer is a pulse of fixed duration established by R_t and C_t.

4. R_t and C_t are the only external components needed.

5. In its stable state, the output of the monostable timer is *low.*

6. The one-shot triggers on a low going pulse.

7. Trigger pulses should be much shorter than the output pulse.

8. P_d min = 20 microseconds. P_d max = 3.6 hours.

9. $V_{th} = \frac{2}{3} V+$.

10. If R_t or C_t is increased, P_d increases.

11. When powered up, the astable (free running) timer produces output pulses. (No triggering)

12. An astable timer has three external components; R_{t_a}, R_{t_b} and C_t.

13. C_t charges through R_{t_a} and R_{t_b}.

14. C_t discharges through R_{t_b} and Q_1.

15. For astable operation, both internal comparators are used.

16. There are two threshold levels; V_{uth}, *which equals* $\frac{2}{3}$ of $V+$ and V_{lth} which equals $\frac{1}{3}$ $V+$.

17. While the capacitor is charging, the output of the timer is *high*; while it is discharging, the output is *low.*

18. Duty factor is the comparision of the time the output is *high* to the total time (period) of the wave.

19. Output *up* time is always greater than *down* time.

20. If C_t increases, t_1, t_2 and period T increase, frequency decreases, and duty factor remains unchanged.

21. If R_{t_b} is increased, t_1, t_2 and period increase, frequency and duty factor decrease.

22. If R_{t_a} is increased, t_1, period and duty factor increase, frequency decreases, and t_2 is unchanged.

23. The 322 is a precision monostable timing device which offers great flexibility due to an internal *ex*-OR logic gate and a floating output power transistor.

24. The output pulse duration of the 322 is equal to 1 $R_t\ C_t$ time constant.

25. The 2240 timer/counter can be configured for monostable or astable operation.

26. The counter section of the 2240 is composed of an 8-bit binary counter which is used to multiply the basic TBO timing pulse by the output ($2T$, $8T$, $64T$ etc.).

8-8 Chapter Progress Evaluation

1. In a 555 monostable timer, what determines the output frequency?

2. Design a monostable timer to produce an output pulse of .22 seconds if C_t equals 1 μF.

3. In a monostable timer, when V_{out} is high, what is the state of:
   a) C_t
   b) Q_1
   c) the comparator
   d) the flip-flop output

4. Referring to an astable timer during t_1, what is the state of:
   a) C_t
   b) Q_1
   c) upper comparator
   d) lower comparator
   e) flip-flop output
   f) timer output

5. Referring to the astable timer during t_2, what is the state of:
   a) C_t
   b) Q_1
   c) upper comparator
   d) lower comparator

- e) flip-flop
- f) timer output

6. What factors effect the output frequency of an astable timer?

7. Design a 322 timer circuit which produces a high output timing pulse of 1.5 seconds when the logic input is held low.

8. What is the effect of triggering the 322 and reversing the logic input level at the same time?

9. Why must diodes be used at the output of an IC timer being used to drive an inductive load?

10. If a 2240 timer counter is configured for monostable operation with an R_t of 100 k and C_t equal to .05 μF, what will the pulse duration be if the output is taken from pin $8T$?

11. What is the effect of tying the $2T$ and $16\ T$ outputs together?

Chapter 9

Regulated Power Supplies

Objectives

Upon completion of this chapter, you should be able to do the following:

- Define regulated power supply terms, such as load and line regulation, and ripple rejection
- Explain the operation of shunt, series-pass, and switching regulator circuits
- Describe the major differences among transistor, op amp, and Norton amp series-pass regulators.
- Explain the operation and list the applications of monolithic regulators, including the 723 user programmable IC regulator

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9-1 Introduction

The term *regulated power supply* indicates that active devices, such as transistors or op amps, are used with or built into unregulated power supplies as control elements. These regulators act as electronic filters that eliminate supply variations to provide constant levels of current, voltage, or power; regardless of changes in AC line voltage, load, or environmental conditions.

Since regulated supplies filter electronically, inductor/capacitor filters are generally not needed, leading to reduced space requirements and cost savings. The stabilized output of a regulated supply allows circuits to operate more precisely, and adjustments in output voltage and current to remain stable.

An ideal power supply would have no output impedance, dissipate no power, and recovers instantly from AC line voltage and load changes with no output deviation. Regulated supplies tend to have low DC (static) impedance as well as low AC (dynamic) impedance at all frequencies, as opposed to systems that use inductor/capacitor filters, whose output impedance increases along with frequency. Low dynamic output impedance reduces or eliminates several power supply problems, such as nonlinear frequency response, ripple contamination, and feedback through the power supply. Power supply performance, in terms of regulation, can be evaluated with the following formulas:

$$\%\ \text{Load voltage regulation} = \frac{V_{\text{out}}\ (\text{no load}) - V_{\text{out}}\ (\text{max load})}{V_{\text{out}}\ (\text{no load})} \times 100 \tag{9-1}$$

$$\%\ \text{Load current regulation} = \frac{I_{\text{out}}\ (\text{shorted}) - I_{\text{out}}\ (\text{min})}{I_{\text{out}}\ (\text{shorted})} \times 100 \tag{9-2}$$

Where I_{out} (min) is the minimum rated current:

% Line voltage regulation (for voltage regulators)

$$= \frac{V_{\text{out}}\ (\text{max}) - V_{\text{out}}\ (\text{min})}{V_{\text{out}}\ (\text{normal line voltage})} \times 100 \tag{9-3}$$

% Line voltage regulation (for current regulators)

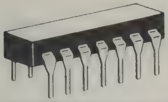
$$= \frac{I_{\text{out}}\ (\text{highest } V_{\text{out}}) - I_{\text{out}}\ (\text{lowest } V_{\text{out}})}{I_{\text{out}}\ (\text{normal line voltage})} \times 100 \tag{9-4}$$

$$\text{Temperature coefficient} = \frac{\%\ \text{change in } V_{\text{out}} \text{ or } I_{\text{out}}}{\text{degree centigrade in ambient temp}} \tag{9-5}$$

Load regulation **is the measure of a power supply's ability to maintain a constant output (current or voltage) under conditions of changing loads.** ***Line regulation*** **is the measure of a power supply's ability to maintain a constant output under changing supply conditions.** ***Average temperature coefficient*** **is an indicator of how changes in temperature will affect the level of output regulation.**

Another term used with regulated power supplies is *ripple rejection.* Regulator circuits are commonly used following rectifier circuits which produce pulsating DC voltages. The ability of the regulator to accept fluctuating voltages and produce a constant DC output is termed *ripple rejection ratio*, and is usually expressed in decibels. When a 1-volt ripple is applied to the input of a regulator circuit, and the ripple is reduced to .001 volt at the output, the ripple rejection ratio is:

$$\begin{aligned} dB &= -20 \log \frac{V_{\text{out}}\ \text{ripple}}{V_{\text{in}}\ \text{ripple}} \qquad (9\text{-}6) \\ &= -20 \log \frac{.001\,V}{1\,V} \\ &= -20 \log\ .001 \\ &= -60\ dB \text{ of ripple rejection} \end{aligned}$$



There are three forms of regulation: *voltage, current,* and *power regulation. Voltage regulators* use current variations to maintain constant levels of output voltage. *Current regulators*, such as the constant current sources and current mirrors discussed earlier, use constant voltage references to supply constant output currents. Current regulated supplies tend to have very poor voltage regulation, and conversely, voltage regulated supplies make poor current regulators. Current and voltage regulators can be combined to produce *power regulators* and overcurrent protected voltage regulators.

There are three types of regulator circuits: *shunt, series-pass,* and *switching.* Each approaches regulation somewhat differently.

Topic Review 9-1

1. The term "regulated power supply" indicates that active devices, such as ______ and ______ ______, are used with or built into unregulated power supplies as control elements.

2. An ideal power supply has no ______ ______, dissipates no power, and recovers instantly from line and load changes, with no ______ deviation.

3. % Load voltage regulation equals ______.

4. Load regulation is the measure of a power supply's ability to maintain a constant ______ (current or voltage) under conditions of changing loads.

5. There are three types of regulator circuits: ______, ______ ______, and ______.

Answers:

1. transistors
   op amps
2. output impedance
   output
3. $$\frac{V_{\text{out}}\,(\text{no load}) - V_{\text{out}}\,(\text{max load})}{V_{\text{out}}\,(\text{no load})} \times 100$$
4. output
5. shunt, series-pass, switching

9-2 Shunt Regulators

The most simple and inexpensive approach to voltage regulation is the use of the reverse-biased breakdown voltage of a zener diode. Its purpose is to maintain a constant value of voltage across the output terminals of a power supply. In **Figure 9-1**, the load is placed in parallel with the zener diode, hence the title *shunt regulator*.

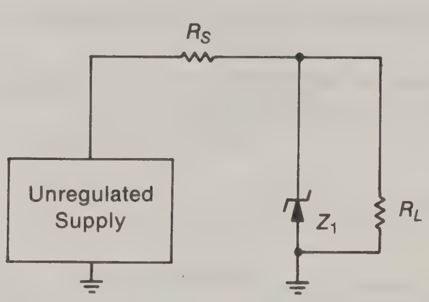


Figure 9-1. Zener shunt regulator

Series resistor R_S is used as an error detector and to limit current through the zener diode.

To understand the operation of the shunt zener regulator, let's first examine the operation of a similar series-parallel resistance network, shown in **Figure 9-2.** If, during normal operation of the circuit, the resistive value of R_L is decreased, the total resistance of the circuit is decreased and total circuit current (I_T) is increased. The result from the standpoint of the load (R_L) is that the load current sustains a permanent increase and the voltage dropped across the load (V_L) permanently decreases.

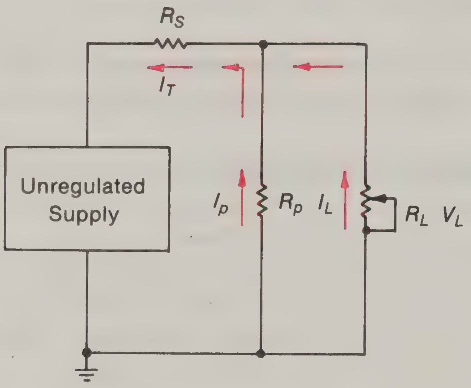


Figure 9-2. Series-parallel resistance network

In contrast, the zener regulator circuit responds to load changes (and supply changes) quite differently.

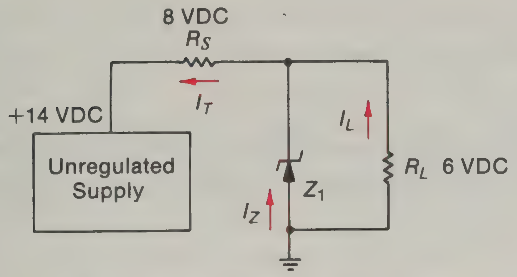


Figure 9-3a. Zener regulator

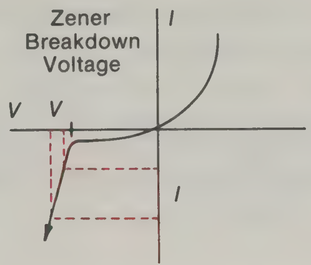


Figure 9-3b. Zener characteristic curve

During normal operation of the circuit shown in **Figure 9-3a**, if the zener is rated to break down at 6 volts, the voltage across the load must also be 6 volts. With the power supply shown, R_S is forced to drop 8 volts.

$$+14V - 6V = 8V$$

If the load varies so that load current tends to increase and load voltage tends to decrease, the voltage across the zener also decreases and current through R_S tends to increase. From the zener diode's characteristic curve, shown in **Figure 9-3b**, it can be seen that a small decrease in zener voltage causes a major decrease in current flow through the zener. The major decrease in zener current causes the current through R_S to decrease, reducing the voltage dropped across it. As the voltage across R_S decreases, the voltage across the zener, and therefore the load, is forced to increase back to the normal operating level. The zener diode regulates the output almost instantaneously, and functions in the same manner for increases in load or power supply voltages.

The value of the sensing resistor must be calculated to fit the design requirements of the regulator. As an example, R_S, in **Figure 9-3a**, must supply both the zener current and the load current, while dropping approximately 8 volts. The zener's operating current should be chosen from its characteristic curve at some value nearly halfway between the knee of the curve and the maximum allowable current. This is done for two reasons. First, poor regulation is obtained when operating near the knee of the curve; and secondly, it allows as much load variation as possible, while still obtaining good regulation and preventing damage to the zener.

If the regulator in **Figure 9-3a** is designed to supply up to 500 mA of load current, and zener current of approximately 50 mA, the necessary value of R_S can be calculated by Ohm's Law.

$$V_{RS} = V_{\text{supply}} - V_Z \tag{9-7}$$

$$V_{RS} = 14V - 6V = 8V$$

$$R_S = \frac{V_{RS}}{I_Z + I_L}$$

$$R_S = \frac{8}{.05 + .5} \tag{9-8}$$

$$R_S = 14.5\Omega$$

Lastly, the power dissipating capability of the zener diode must be considered. Normal operation of the regulator will call for the zener to dissipate power as shown below.

$$P_D = V_Z \times I_Z \tag{9-9}$$

$$P_D = 6V \times 50\ mA$$

$$P_D = .3W$$

In a different situation, such as an open load, the zener is forced to carry all of the circuit current. The power dissipation of the zener in this case would be:

$$P_D = V_Z \times I_T \tag{9-10}$$

$$P_D = 6 \times 550\ mA$$

$$P_D = 3.3W$$

The zener's power rating should be twice this level to insure reliable operation of the circuit. Therefore, the zener diode should be rated to dissipate at least 7 watts in **Figure 9-3.**

In **Figure 9-4**, an active device (*Q*) is used as a variable resistance in parallel with the load. The voltage divider formed by *Z* and *R* provides biasing for the shunt transistor and acts as the error detector for the circuit.

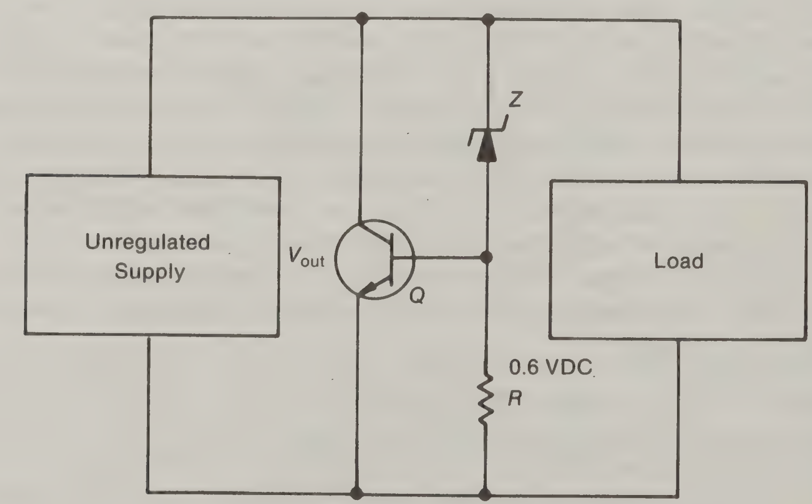


Figure 9-4. Zener regulator with active device

If the output voltage attempts to increase, the voltage across the zener diode increases, causing an increase in zener current. The increased current flow in the voltage divider causes the voltage drop across the resistor to increase, increasing the forward bias on the base-emitter junction of Q_1. This causes increased emitter to collector current flow, and decreased voltage across the transistor, opposing the increased load voltage. Any change in load condition or power supply voltage is detected by the voltage divider, and adjusts the bias level on the base of the transistor. The output voltage level is established by the sum of the voltage drops across R_1, and the breakdown voltage of the zener.

$$V_{out} = V_Z + V_{R1} \tag{9-11}$$

V_R is equal to the voltage drop across the base-emitter junction of the transistor.

$$V_{R1} = V_{BE} = 0.6V \tag{9-12}$$

A major drawback of shunt-type regulators is that large amounts of standby current must flow through the circuit at all times. This results in excessive power consumption and limits the use of shunt regulators to low power applications.

Topic Review 9-2

1. In a shunt regulator, the load is placed in ______ with the zener diode.
2. In **Figure 9-3a**, a small decrease in zener voltage causes a major ______ in current flow through the zener.
3. The zener's operating current should be chosen from its characteristic curve at some value halfway between the ______ and the maximum allowable ______.
4. The zener's power rating, in any shunt-regulated circuit, should be ______ the calculated power dissipation of the zener.
5. A major drawback to shunt regulators is their excessive ______ ______.

Answers:

1. parallel
2. decrease
3. knee
   current
4. twice
5. power consumption

9-3 Series-Pass Regulators

A *series-pass regulator* uses an active control element as a variable resistance in series with the load. Any change in power supply or load condition causes the control element to adjust the output current. This offsets the change and maintains a constant load voltage.

Series-pass regulators offer lower levels of power dissipation than the shunt type, because the circuit doesn't require large values of quiescent current. For this reason, series regulators are more common in medium and high-power applications.

Figure 9-5 shows a simple series-pass regulator circuit. The load current passes and is controlled by, the pass transistor (Q_1).

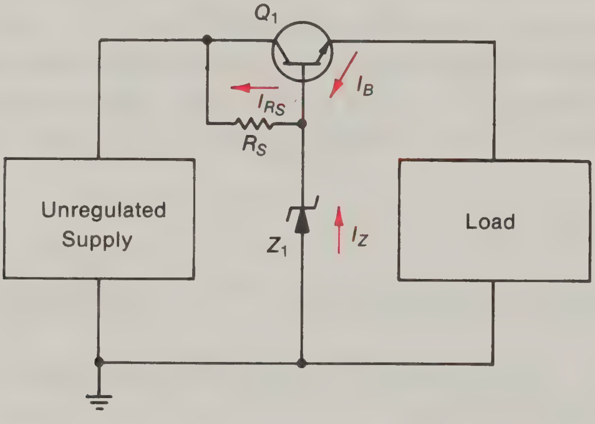


Figure 9-5. Simple series-pass regulator circuit

The zener diode (Z_1) establishes a reference voltage on the base of the pass transistor (Q_1). The output voltage is determined by the zener voltage minus a base-emitter voltage drop.

$$V_{\text{out}} = V_Z - 0.6V \qquad (9\text{-}13)$$

If the load varies so that the load voltage tends to increase, the forward bias on the base-emitter junction is decreased. This causes Q_1 to conduct less current and drop more of the supply voltage, opposing the output voltage increase. Conversely, if the load voltage tends to decrease, the forward bias (Q_1) increases. Thus, the transistor conducts harder and drops less of the source voltage.

Supply changes are detected by the zener/resistor voltage divider. Resistor R_S limits current to the zener diode and the base of the transistor.

$$I_{R_S} = I_Z + I_B \qquad (9\text{-}14)$$

If the power supply voltage increases, current through the zener and R_S increases, causing R_S to drop more of the source or supply voltage.

A series-pass regulator can also be constructed to provide variable levels of regulated output voltage, by incorporating a variable voltage divider, as shown in **Figure 9-6**.

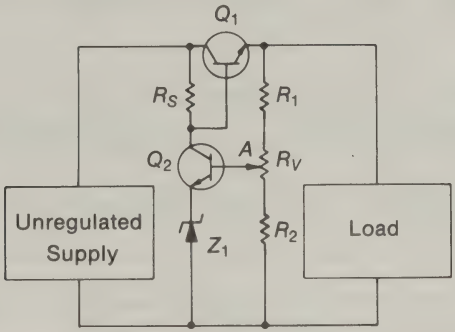


Figure 9-6. Variable voltage series-pass regulator

The resistive voltage divider acts as an error detector at the regulator output. The voltage divider establishes the biasing of the sensing device, Q_2. Z_1 sets the reference voltage on the emitter of Q_2. Q_2 is used to control the series-pass transistor, Q_1.

If the output voltage attempts to increase, the increase is detected across the resistive voltage divider at point A. The increase of point A causes Q_2 to conduct more current. This causes resistor R_S to drop more of the source voltage, decreasing the collector voltage of Q_2, and therefore the base voltage of Q_1. The pass transistor conducts less current, dropping more of the source voltage, and opposing the output voltage increase.

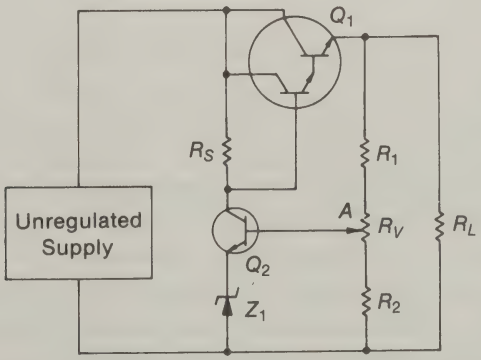


Figure 9-7. Variable voltage series-pass regulator with Darlington transistor

The efficiency of this regulator is improved by replacing pass transistor Q_1 with a Darlington configuration, as shown in **Figure 9-7**. The extremely high gain of the Darlington makes the circuit more sensitive to change, which provides closer output regulation.

Topic Review 9-3

1. A series-pass regulator uses an active control element as a ______ ______, in series with the load.

2. A series-pass regulator can be constructed to provide ______ levels of regulated output voltage, by incorporating a ______ voltage divider in parallel with the load.

3. The resistive voltage divider, in **Figure 9-6**, acts as an ______ ______ at the regulator output.

4. In **Figure 9-5**, the output voltage is determined by the ______ voltage minus the ______ - ______ voltage drop of Q_1.

5. The efficiency of the series-pass regulator, in **Figure 9-6**, can be improved by replacing pass transistor Q_1 with a ______-type transistor.

Answers:

1. variable resistance
2. variable
   variable
3. error detector
4. zener
   base-emitter
5. Darlington

9-4 Op Amp Regulators

Voltage regulators using transistors as sensing devices offer some good regulation features, but they also tend to have low sensitivity and slow response time. In many applications, these conditions cannot be tolerated.

These drawbacks can be overcome quite easily by replacing the sensing transistor with an operational amplifier. The op amp senses changing conditions, detects errors, and provides a correction signal much quicker than a simple transistor. These abilities are due to the highly sensitive nature of the op amp's input terminals. Therefore, an op amp in a voltage regulator circuit may be referred to as an error amp.

An op amp configured as a noninverting amplifier is shown in **Figure 9-8**. Since the output voltage of an op amp is determined by the ratio of an external resistor network, the op amp makes a fairly good voltage regulator on its own, provided a

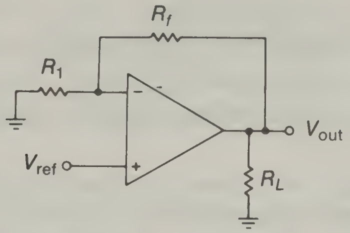

R_f
R_1
V_{out}
V_{ref}
R_L

Figure 9-8. Simple op amp regulator

constant level of input voltage is maintained at V_{ref}.

The output voltage is determined by the formula:

$$V_{out} = \left(\frac{R_f}{R_1} + 1\right)V_{ref} \tag{9-15}$$

As shown in **Figure 9-9**, a zener diode is used to maintain a constant level of voltage for V_{ref}. The level of output voltage is made variable by the use of a potentiometer, to replace both R_1 and R_f.

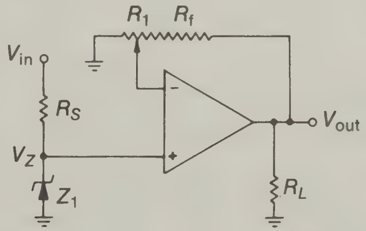

R_1 R_f
V_{in}
R_S
V_{out}
V_Z
Z_1
R_L

Figure 9-9. Variable output op amp regulator

The major drawback of this circuit is that the op amp doesn't have the output current capabilities to perform as much useful work as a regulating power supply. However, the op amp is most useful when used to control a series-pass transistor (figure 9-10). Now the output current is limited only by the size of the pass transistor.

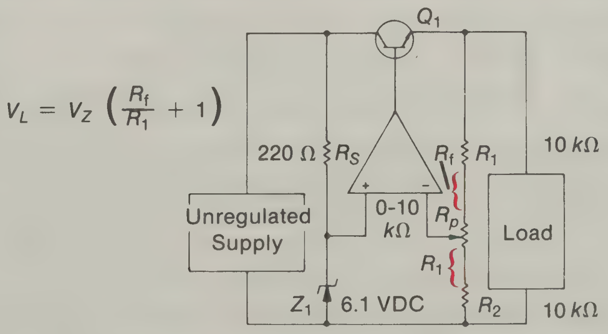

$$V_L = V_Z\left(\frac{R_f}{R_1} + 1\right)$$
Q_1
220 Ω
R_S
R_f
R_1
10 kΩ
Unregulated Supply
0-10 kΩ
R_p
Load
R_1
Z_1
6.1 VDC
R_2
10 kΩ

Figure 9-10. Op amp controlled series-pass regulator

Reference voltage is established by voltage dividers R_S and Z_1 on the non-inverting input of the op amp. The output voltage of the regulator is equal to the output voltage of the op amp, minus V_{BE} of the pass transistor. Potentiometer R_p allows the output voltage to be adjustable, by varying the ratio of the feedback voltage divider.

Once the output voltage level has been established, any attempted change in load voltage will be felt across the voltage divider. This causes the op amp output to swing in the opposite direction (−input) and vary the current through Q_1, which is required to maintain constant output voltage.

In the event of a current overload, it is desirable to have some means to quickly protect the circuit. Fuses tend to be too slow, so overcurrent protection must be done electrically. A current limited, voltage regulated power supply is shown in **Figure 9-11.**

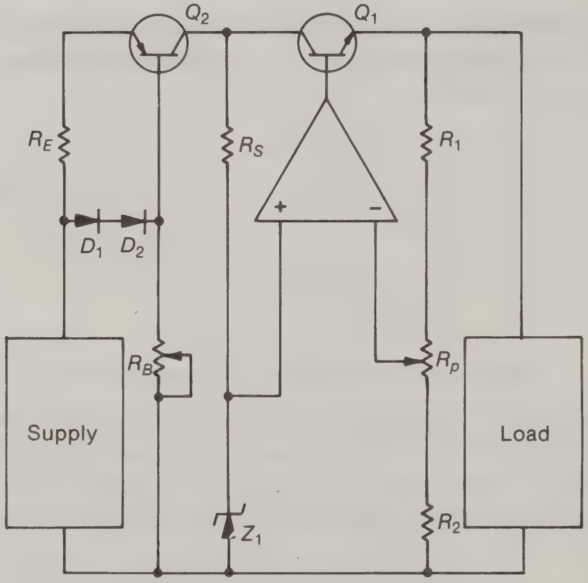


Figure 9-11. Current limited series-pass regulator

Diodes D_1 and D_2, resistors R_B and R_E, and PNP transistor Q_2 are added to the op amp voltage regulator to provide current limiting. Resistor R_E is a small resistance value, calculated to drop 0.6 volts at maximum desired output current. Potentiometer R_B is adjusted until transistor Q_2 begins to saturate $I_{out(\max)}$. Diodes D_1 and D_2 limit the amount of voltage that can be dropped across R_E, and the base-emitter junction of Q_2, to approximately 1.2 volts. If the current through R_E attempts to increase, so that R_E is forced to drop more than 0.6 volts, the diodes conduct and clamp the base of Q_2. Therefore, the transistor is prevented from conducting more current.

$$R_E = \frac{0.6V}{I_{\text{out (max)}}} \text{ (desired)} \tag{9-16}$$

Norton amplifiers are also used as control elements in series-pass regulator circuits.

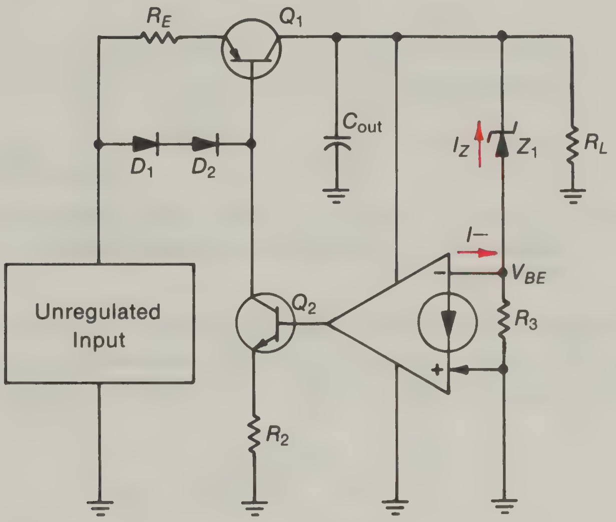


Figure 9-12. Norton amplifier voltage regulator

The Norton amp configuration, shown in **Figure 9-12**, uses NV_{BE} biasing with feedback provided by Z_1. The voltage across R_3 is held constant at 0.6 volts by the Norton inverting input.

Should the load vary so that the output voltage tends to increase, the increased voltage is felt across the zener, causing the current leaving the inverting input to increase. This causes the Norton's output to swing negative, cutting back the current flow through transistor Q_2. As Q_2's collector voltage decreases, the base voltage of Q_1 swings positive, causing Q_1 to conduct less, dropping more of the source voltage and offsetting the output voltage increase. The circuit responds in reverse to attempted decreases in load voltage. Current limiting is again provided by R_E, and diodes D_1 and D_2. The capacitor across the output protects the power supply from high-frequency transients.

The output voltage of this configuration is limited to the voltage rating of the zener diode, plus the voltage dropped across R_3, which is held at 0.6 volts by the Norton amplifier.

$$V_{\text{out}} = V_Z + V_{BE} \tag{9-17}$$

The output voltage of the Norton amp regulator is increased by reconfiguring the circuit slightly, as shown in **Figure 9-13.**

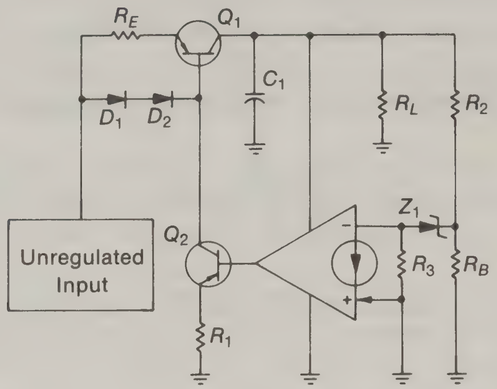


Figure 9-13. Norton amplifier voltage regulator with increased V_{out}

The output voltage is now determined by the zener rating, V_{BE}, and the voltage dropped across R_2. The value of the output is determined by examining the voltage divider, where R_3 is in parallel with $V_Z + V_{BE}$. To find V_{out}, begin with:

$$V_Z + V_{BE} = \frac{R_3}{R_2 + R_3\,(V_{out})}$$

then:

$$V_{out} = \frac{V_Z + V_{BE}}{\dfrac{R_3}{R_2 + R_3}}$$

finally:

$$V_{out} = \frac{R_2 + R_3}{R_3}(V_Z + V_{BE}) \qquad (9\text{-}18)$$

Topic Review 9-4

1. The drawbacks of a transistor, in a series-pass voltage regulator, can be overcome by the use of an ________ ________ .
2. However, a certain disadvantage exists. There is a limited ________ capability.
3. The best use of an op amp, in a series-pass voltage regulator circuit, is in its ability to control the base current of a ________-________ ________ .
4. In **Figure 9-11**, D_1 and D_2, R_E, R_B, and Q_2 are added to provide ________ limiting.
5. In **Figure 9-13**, V_{out} equals ________ .

Answers:

1. operational amplifier
2. current
3. series-pass transistor
4. current
5. $\frac{R_2 + R_3}{R_3}(V_Z + V_{BE})$

9-5 Switching Regulators

A somewhat different approach to regulation is shown in **Figure 9-14**. This configuration is a DC switching power supply.

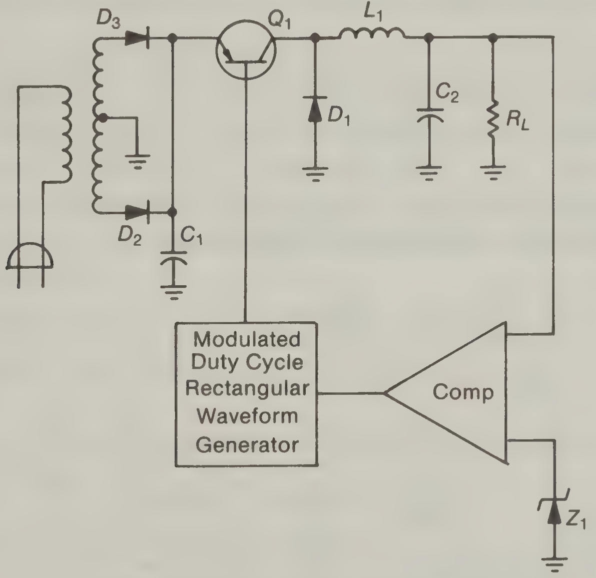


Figure 9-14. DC switching power supply

The major difference between the switching-type supply and the types of regulators covered so far is in the operation of the active control device. The previous regulators used the active device as a variable resistance to maintain constant levels of output voltage, causing the control element to dissipate power at all times. The *switching regulator*, by comparison, controls output voltage by using a pass transistor as a variable duty-cycle switch to produce an average DC collector voltage. Since the transistor is cut off, preventing current flow for a portion of time, the switching regulator consumes much less power than the shunt and series-pass regulators, producing a more efficient power supply.

An op amp comparator is used to detect any difference between the circuit's output voltage and the reference voltage developed by Z_1, and to produce an error voltage which is applied to the duty-cycle modulator. The action of the duty-cycle modulator, or pulse-width modulator, is similar to the astable timer (described in Chapter 8), with the voltage control terminal used to vary the duty cycle of its output.

Pulse-width modulators (PWM) are available in IC form. The LM 1524 series PWM provides all the circuitry necessary to control switching regulators of either polarity. Since Q_1 is a PNP transistor, the duty cycle of the modulator must be inverse to the duty cycle of the transistors output. In other words, the longer the output of the modulator is low, the longer the output of Q_1 is high. The average DC voltage is applied to the low pass filter formed by L_1 and C_2, which converts the average voltage to a pure DC voltage. Capacitor C_1 is used to provide prefiltering. Diode D_1 is a freewheeling diode which allows the inductor to discharge when the transistor is cut off, maintaining constant current direction through the load at all times.

Switching regulators do not generally possess the close regulation qualities of dissipative type regulators. For this reason, switching regulators are often used as pre-regulators for dissipative regulators, realizing the best qualities of both types of regulators.

Switching regulators can also be used to provide stepped up output voltages. A step-up switching regulator is shown in **Figure 9-15.**

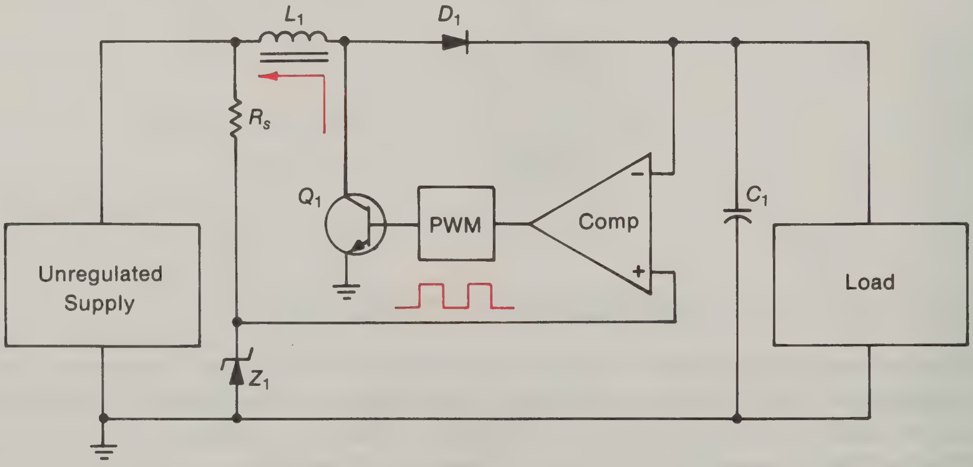


Figure 9-15. Step-up switching regulator

When Q_1 is turned on, a portion of the current flows into L_1, developing a counter EMF in the inductor. When the pulse-width modulator turns Q_1 off, the field in the inductor collapses. This induced voltage appears to the load to be series aiding with the unregulated supply voltage. Therefore, the load sees a stepped-up output voltage.

Diode D_1 keeps the filter capacitor (C_1) from discharging while Q_1 is turned on. As was the case with the previous switching regulator, output regulation is controlled by a reference voltage, an error amplifier, and a pulse-width modulator.

As a note of caution when working with switching regulators, it should be stressed that proper test equipment and safe work habits are a must. Inductive kickback, due to the switching action, can produce deadly voltage levels, even in low-voltage regulators.

Switching regulator subsystems, which supply most of the components necessary for switching regulator systems, are available in IC form. An example of these circuits is the μA 78540 universal switching regulator subsystem. This IC consists of a temperature compensated reference voltage, an error amp, a high-current/high-voltage output switch, a power diode, and a duty-cycle controlled oscillator with an active current limiter.

Topic Review 9-5

1. Switching regulators provide ______ efficiency and ______ power dissipation.
2. Switching regulators do not have the high degree of ______ found in series-pass and shunt-type regulators.
3. In **Figure 9-14,** an ______ ______ comparator is used to detect any difference between the circuit's output voltage and the reference voltage.
4. In **Figure 9-14**, the action of the duty-cycle modulator is very similar to an ______ multivibrator or timer.
5. Switching regulators can also be used as ______ - ______ for dissipative regulators, and as ______ - ______ voltage regulators, as in **Figure 9-15.**

Answers:

1. high
   low
2. regulation
3. op amp
4. astable
5. pre-regulators
   step-up

9-6 Three-Terminal Regulators

IC manufacturers produce a line of easy-to-use, fixed-voltage regulators, referred to as *three-terminal regulators*. These devices are available in a limited number of both positive and negative output voltages, some with current capabilities greater than 1.5 amps. From **Figure 9-16**, it can be seen that three-terminal regulators are very similar to the discrete op amp regulators previously discussed.

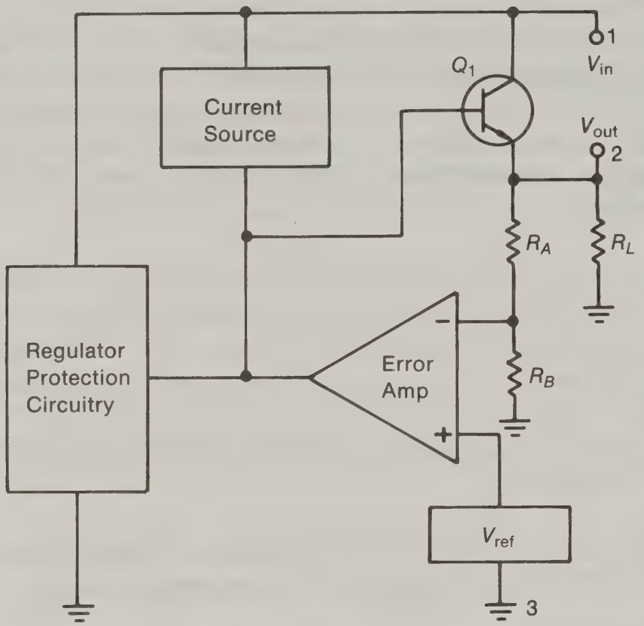


Figure 9-16. Typical three-terminal regulator

The op amp error detector senses any deviation between the output voltage and the internally generated reference voltage, and adjusts the series-pass transistor biasing. This maintains the regulators constant output voltage at the rated value.

Three-terminal regulators provide internal short circuit and thermal overload protection. The protection circuitry is designed to protect the regulator only, and may not protect the load or power supply in overcurrent situations.

When designing circuits using three-terminal regulators, there are two factors that must be taken into account. These are the unregulated supply voltage and the desired output voltage. **Typically, the supply voltage must be at least 2 volts greater than the desired output voltage, due to the minimum internal voltage drop of the regulator.** This is termed *drop-out voltage*. The output current requirements of the regulated circuit must be estimated and checked against the manufacturer's data sheet. The last factor to be considered is the heat sink requirement of the voltage regulator.

A three-terminal regulator is used with a current-boost transistor to produce a high-current output voltage regulator, as shown in **Figure 9-17**.

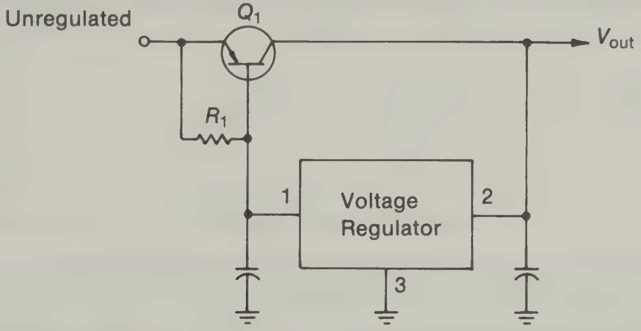


Figure 9-17. High-output current voltage regulator

This fixed regulator is capable of supplying current of up to 150 mA. When more current is required, resistor R_1 forward biases the base-emitter junction of Q_1, supplying increased output current. The point at which the current-boost transistor turns on is determined by the size of R_1, which can be calculated by:

$$R_1 = \frac{V_{BE}}{I_{out}\ \text{(desired)}} \tag{9-19}$$

As an example, in order to turn on Q_1 when the output current exceeds 100 mA, resistor R_1 must be:

$$R_1 = \frac{.7V}{100\ mA}$$

The output current is limited only by the current capabilities of Q_1.

A variable regulated output voltage is achieved by configuring the three-terminal regulator, as shown in in **Figure 9-18.**

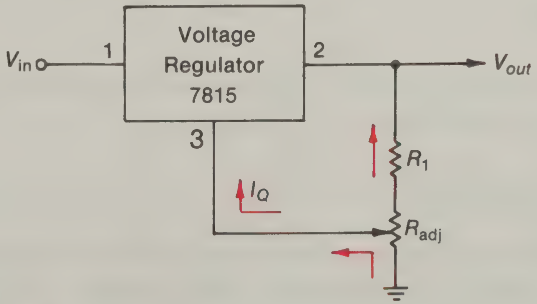


Figure 9-18. Variable output voltage regulator

The rated voltage of the regulator is imposed across resistor R_1 of the output voltage divider, which established the voltage divider current. This current is added to the regulators quiescent current and flows through R_{adj}. The output voltage is calculated by the formula:

$$V_{\text{out}} = V_{\text{reg}} \left(\frac{R_{\text{adj}}}{R_1 + R_{\text{adj}}}\right) + (I_Q R_{\text{adj}})$$

$$V_{\text{out}} = V_{\text{reg}} \left(1 + \frac{R_{\text{adj}}}{R_1}\right) + (I_Q R_{\text{adj}}) \tag{9-20}$$

The voltage divider current should be at least ten times greater than I_Q.

A regulated current source is shown in **Figure 9-19**. The rated voltage of the regulator is imposed across R_1, establishing a constant output current. This current is added to the manufacturers specified output current, I_Q. I_{out} is determined by:

$$I_{\text{out}} = \frac{V_{\text{reg}}}{R_1} + I_Q \tag{9-21}$$

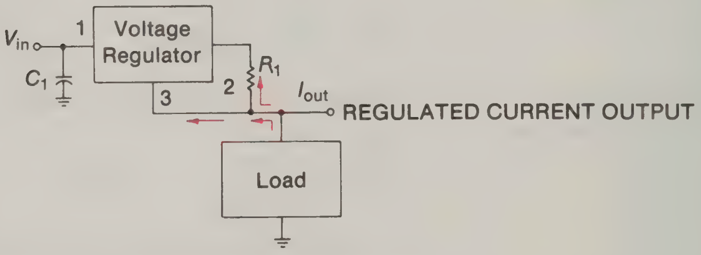


Figure 9-19. A three-terminal regulator implemented as a current regulator

Topic Review 9-6

1. IC manufacturers produce a line of easy-to-use, monolithic voltage regulators, called ______ ______ regulators.

2. These regulators come in both ______ and ______ fixed voltages.

3. The only requirement when using three-terminal regulators is that the input voltage be at ______ volts ______ than the stated output voltage. This is called the drop-out voltage.

Answers:

1. three-terminal
2. positive
   negative
3. 2
   greater

9-7 Programmable 723 Voltage Regulator

For IC applications where the power supply voltages required are not available in a simple three-terminal regulator, *the 723 user programmable voltage regulator* proves to be a very versatile device. The 723 can be programmed by external resistor combinations to provide either positive or negative voltage regulation from 2 to 37 volts DC, with output currents up to 150 *mA*. Overcurrent protection is also user programmable.

The block diagram of the 723, in **Figure 9-20,** reveals that the 723 operates similar to the discrete op amp voltage regulators discussed earlier in this chapter.

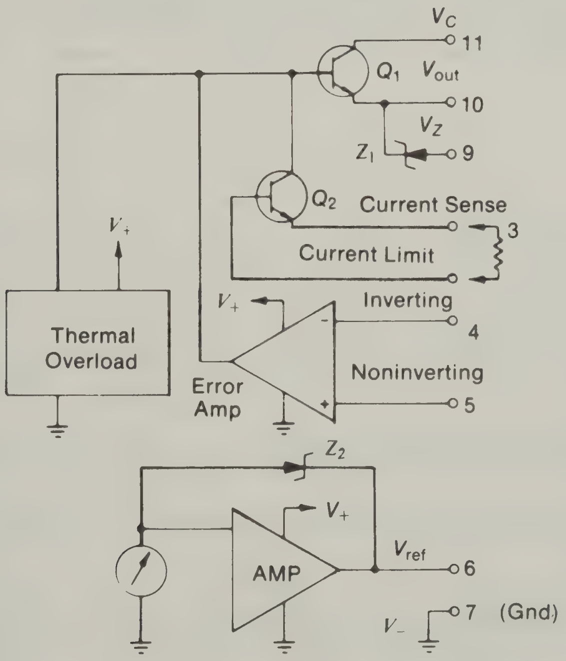

V_C
11
Q_1
V_{out}
10
V_Z
Z_1
9
Q_2
Current Sense
3
Current Limit
V_+
Inverting
4
V_+
Thermal Overload
Error Amp
Noninverting
5
Z_2
V_+
AMP
V_{ref}
6
V_-
7 (Gnd)

Figure 9-20. Internal equivalent diagram of the 723 voltage regulator

The 723 develops its own temperature compensated reference voltage internally across Z_2. The error amp is used to compare the reference voltage to the output voltage. The difference between the two is amplified and applied to the base of pass transistor Q_1. The error voltage increases or decreases the emitter current of Q_1, to hold the output voltage constant. Transistor Q_1 is actually a Darlington pair and the output current is very high. For this reason, the output current should be limited to 150 mA. An external-pass transistor can be added if greater output current is desired.

Transistor Q_2 provides overcurrent protection which is user programmable. An external resistor is connected across the base-emitter junction of Q_2. When the current through R_{CS} causes V_{RCS} to exceed 0.6 volts, Q_2 turns on and shorts the base of Q_1 to ground, cutting off the output current. The value of resistor R_{CS} is calculated by the formula:

$$R_{CS} = \frac{0.6V}{I_{\text{limit}}} \tag{9-22}$$

On the other hand, the thermal overload circuitry is internal, and therefore not user adjustable.

The 723 manufacturer supplies easy-to-use, standardized circuit configurations for positive 2 to 7 volt regulation, positive 7 to 37 volt regulation, negative regulation, positive and negative switching regulation, and high current output regulation. The manufacturer also provides a table of suggested resistor values for the above configurations.

TABLE I RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGE

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	-6 (Note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	-9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	-12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	-15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	-28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	-45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	-100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	-250	8	3.57	249	2.2	10	240

Courtesy of National Semiconductor

For regulated voltage outputs not listed in the table, resistance values must be interpolated. *Interpolation* is a logical process of determining intermediate values from a table by examining the magnitude and direction of the changing values. As an example, let's design a +10 volt regulated supply with output current limited to 100 *mA*.

The first step is to pick the correct circuit configuration, which in this case is the manufacturers suggested configuration, for output voltages between +7 and +37 volts. The value of R_{CS} is calculated to be:

$$R_{CS} = \frac{.7V}{100\ mA}$$

Next, the values of R_1 and R_2 are interpolated from the table of resistor values.

The value of +10 volts is $\frac{1}{3}$ of the distance between the standard values of +9 and +12 volts. The value of R_1 increases from 1.87 $k\Omega$ to 4.87 $k\Omega$, between +9 and +12 volts, which indicates that R_1 will increase by $\frac{1}{3}$ for a +10 volt output.

$$\text{therefore:}\ R_1 = 2.87\ k\Omega$$

The value of R_2 does not change between +9 and +12 volts, so $R_2 = 7.15\ K\Omega$.

$$\text{next,}\quad R_3 = \frac{R_1\ R_2}{R_1 + R_2}$$

$$\text{then,}\quad R_3 = 2.04\ k\Omega$$

At this point we have calculated the necessary values to operate a +10 VDC regulated supply at a limited current of 100 *mA*.

9-8 Summary Points

1. Regulated power supplies use active elements to electronically filter out variations in the output.
2. Voltage regulators vary current to maintain constant levels of output voltage.
3. Current regulators allow voltage to vary in order to maintain constant output current.
4. Current regulators have poor voltage regulation. Voltage regulators have poor current regulation.
5. Voltage regulators fall into three categories: shunt, series-pass and switching.

6. Shunt regulators use an active control element in parallel with the load.

7. Series-pass regulators use a pass transistor as a variable resistance in series with the load.

8. Switching regulators use the active control element as a variable duty-cycle switch, either in series or parallel, with the load.

9. Shunt regulators are limited to low power applications, because large currents flow through the circuit at all times.

10. Series-pass regulators may use zener diodes, transistors, or op amps as sensing devices to control a high-current pass transistor.

11. Op amps can be used as voltage regulators, however, the current output capabilities of the op amp are too low for it to ideally control output voltage on its own.

12. Switching regulators provide high efficiency, low power dissipation regulation, because current flows through the circuit for only a portion of the time. Switching regulators do not have the high degree of regulation found in series and shunt-type regulators.

13. Most of the components necessary to construct a switching regulator are available in single IC form.

14. IC manufacturers produce a line of easy-to-use, monolithic voltage regulators, called three-terminal regulators.

15. Three-terminal regulators operate with both positive and negative fixed voltages.

16. The only requirement when using three-terminal regulators is that the input voltage be approximately 2 volts greater (drop out voltage) than the stated output voltage. Heat sinking may be required in some applications.

17. With the addition of a few external components, these regulators may be configured to perform many diverse functions. Addition of any external components to three-terminal regulators degrades the high regulation qualities of the devices.

18. A current regulator can be constructed with a three-terminal regulator, an op amp, or simply a transistor constant current source.

19. The 723 user programmable voltage regulator can be configured as a positive, negative, switching, or high-current voltage regulator, with current limiting programmed by the user.

9-9 Chapter Progress Evaluation

1. What is the regulation performance, in percent, of a power supply with a no load voltage of +14 VDC, and a maximum load voltage of 10 VDC?

2. What is the ripple rejection, in *dB*, of a power supply that has an input ripple voltage of 1 volt ripple, and an output ripple that has been reduced to 1 *mV*?

3. In **Figure 9-3a**, if V_Z equals 6 VDC, the supply equals 14 VDC, and R_L equals 360 Ω, what is the current through R_S, if R_S equals 10 Ω?

4. In **Figure 9-3a**, if the regulator is to supply up to 1 ampere of load current, and a zener current of 100 *mA*, what is the value of R_S? Assume that V_Z equals 8 VDC, and V_{supply} equals 16 VDC.

5. What is the power dissipation (P_D) of the zener in **Figure 9-3a**, if V_Z equals 8 VDC and I_T equals 750 *mA*? What is the rating of the zener for safe power supply operation?

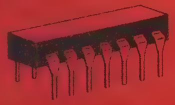
6. In **Figure 9-5**, if V_{supply} equals 14 VDC and V_Z equals 6 volts, what is the voltage drop (V_L) across the load?

7. What is the value of I_{R_S} in **Figure 9-5**, if I_B equals 10 *mA* and I_Z equals 50 *mA*?

8. If V_Z, in **Figure 9-10,** equals 3.9 VDC, R_f equals 10 *k*Ω, R_2 equals 10 *k*Ω, and R_p is adjusted for 5 *k*Ω, calculate V_L.

9. Calculate V_{out} in **Figure 9-18**, if V_{reg} equals 15 VDC, R_1 equals 1 *k*Ω, R_{adj} is a 500 Ω potentiometer set at 250 Ω and I_Q equals 1 *mA*.

10. What must be the external value of resistor R_{CS} in **Figure 9-20**, if the current limit is not to exceed 50 *mA*?



Chapter 10

Phase-Locked Loops

Objectives:

Upon completion of this chapter, you should be able to do the following:

- Describe basic PLL circuit operation
- Design a simple PLL and calculate bandwidth, frequency, capture, and lock ranges
- Explain the internal operation of the 565 PLL IC and list its applications

10-1 Introduction

The phase-locked loop (PLL) is a feedback loop system, whose output locks onto an input frequency signal, and tracks or follows any change in the input frequency. It consists of three basic stages: a phase detector or comparator, a low-pass filter/integrator, and a voltage-controlled oscillator (VCO). The output signal of the VCO is fed back to the input phase detector stage. A block diagram is shown in **Figure 10-1.**

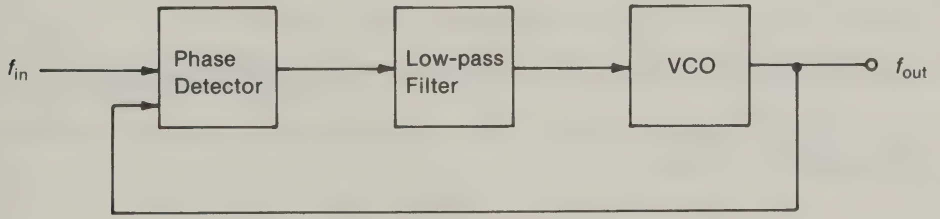


Figure 10-1. A typical PLL block diagram

The phase detector stage compares the frequency of the input signal, f_{in}, to the frequency of the VCO output, f_{out}, and generates a DC error voltage that is proportional to the phase difference of the two. The loop filter removes any noise from the phase detector output and allows the passage of a DC error voltage from the phase detector to the VCO. The output frequency of the VCO stage provides the output frequency of the PLL and also the feedback signal to the phase detector. Its output frequency is a function of its input signal voltage level, and is in essence a voltage-to-frequency converter.

The phase-locked loop, or PLL, has three distinct modes of operation. They are the free-running mode, the capture mode, and the phase-locked or tracking mode. If the VCO output frequency is so far from the input frequency that the PLL cannot lock in the VCO, the loop is in the free-running mode. When the output of the filter stage causes the frequency of the VCO to change, the loop is in its capture mode. Once the loop has captured a signal frequency, the filter output will cause the VCO frequency to change until it matches the input frequency. The loop is then said to be in lock mode or phase-locked. The *lock range* is the frequency range over which the phase-locked loop can follow the incoming signal. The *capture range* is the bandwidth over which capture is possible. The capture range cannot exceed the lock range and is held narrower than the lock range by the phase detector.

It is common, when working with phase-locked loops, to specify phase difference in radians rather than degrees. One cycle of a wave is equal to 360° or 2π radians. To convert from degrees to radians, divide the number of degrees by 57.3. To convert radians to degrees multiply by 57.3:

$$\text{Radians} = \frac{\text{Degrees}}{57.3}$$

$$\text{or: Degrees} = \text{Radians}\,(57.3)$$

Throughout this chapter, the Greek letter ω (omega) is used to specify the frequency in radians/second. This is common to phase-locked loop terminology. The relationship between radian frequency and cycles per second (*Hz*) is expressed mathematically as:

$$\text{Radian frequency}\ (\omega) = 2\pi f$$

Now, let's look in detail at each of the stages of the phase-locked loop.

Topic Review 10-1

1. The phase-locked loop is a feedback loop system whose ________ locks onto an input frequency signal and ________ any change in the input frequency.

2. The three basic stages of the PLL are: a ________ ________, a ________-________ ________ and a ________-________ ________.

3. The PLL has three distinct modes of operation. They are the ______-______ mode, the ______ mode, and the ______-______ mode.

4. The ______ ______ is the frequency range over which the phase-locked loop can follow the incoming signal.

5. The ______ ______ is the bandwidth over which capture is possible.
6. Frequency, specified in ______/______ is common to phase-locked loop terminology.

Answers:

1. output, tracks
2. phase detector, low-pass filter, voltage-controlled oscillator
3. free-running, capture, phase-locked
4. lock range
5. capture range
6. radians/second

10-2 The Phase Detector

All *phase-locked loop* circuits use a phase detector or phase comparator stage. Phase detectors are either the analog or digital type. The phase detector used depends on what type of application for which the phase-locked loop is intended. Generally, analog application of the PLL use a detector called a double-balanced mixer, while digital applications employ an exclusive-OR gate comparator, or an edge-triggered flip-flop comparator.

The term *phase* refers to the length of time between the occurrence of two related events; such as the time interval between two out-of-phase signals crossing zero or some other common point of reference. Phase difference then, is the time between two related events, expressed in degrees or radians. In electrical degrees, phase difference is expressed as leading or lagging.

The symbol for phase difference is $\Delta\phi$, which, when expressed in radians is:

$$\frac{t_2 - t_1}{T} \times 2\pi \tag{10-1}$$

where: T = time
$t_2 - t_1$ = difference in time between intervals

or when expressed in degrees is:

$$\frac{t_2 - t_1}{T} \times 360^\circ \tag{10-2}$$

The function of the phase detector is to produce an average DC error voltage that is proportional to the phase difference between the input and feedback signals.

Phase detector conversion gain (K_D) is the factor that converts phase difference into voltages. The phase detector output voltage is determined as follows:

$$V_{out} = K_D \, \Delta\phi \qquad (10\text{-}3)$$

where: V_{out} is the phase detector output voltage
K_D is the phase detector conversion gain in volts/radian (V/rad)
$\Delta\phi$ is the input phase difference in radians (rad)

A type of phase detector used in digital applications, is the exclusive-OR gate. It produces the following truth table, and its symbol is shown in **Figure 10-2.**

Input A	Input B	Output X
0	0	0
1	0	1
0	1	1
1	1	0

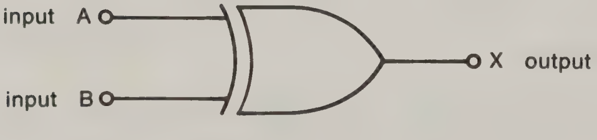


Figure 10-2. Exclusive-OR gate symbol

The zeros represent digital lows (0 volts), and the ones represent a high or turned-on state. Exclusive-OR phase detectors are used for input and feedback waveforms that have a 50% duty factor. **Figure 10-3** shows an exclusive-OR gate and its output waveform, for two signals 90° out-of-phase (or $\pi/2$ radians).

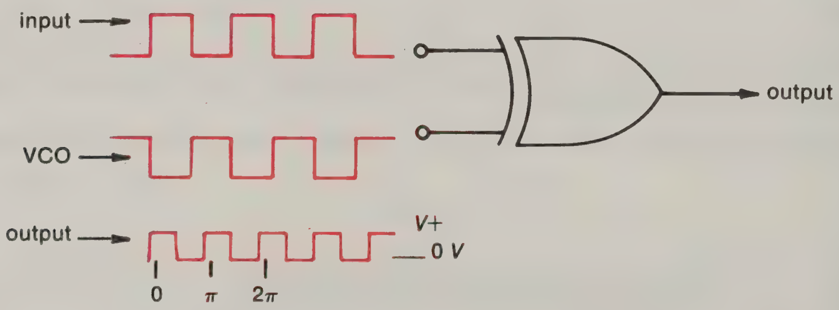


Figure 10-3. Signals $\frac{\pi}{2}$ or 90°, out of phase

From the inputs shown, it can be seen that the output of the ex-OR will be high any time one input is high and the other input is low. The two input signals are $\pi/2$ radians out-of-phase and produce an output signal frequency which is twice the input, with a duty factor of 50%. Therefore, the average value of the output signal is ½ $V+$.

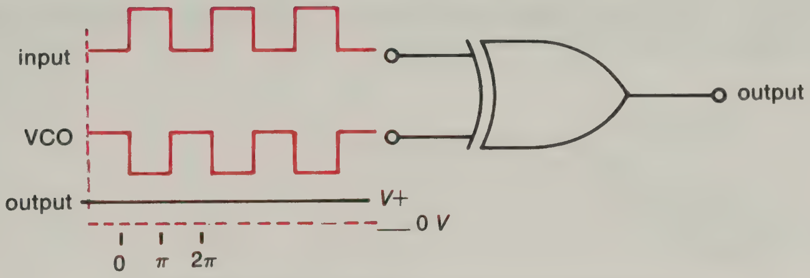


Figure 10-4. Signals π, or 180°, out of phase

As shown in **Figure 10-4**, as the phase shift increases to π radians, the "average value" of the output voltage increases to $V+$. As the phase difference increases further, the average output voltage will begin to decrease.

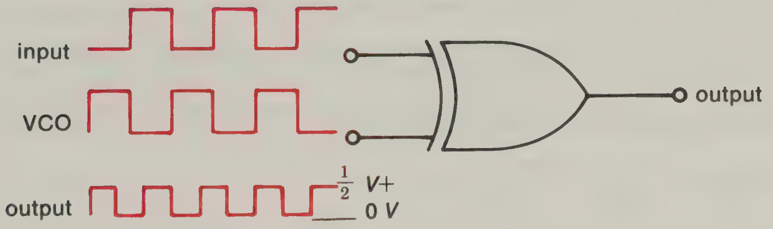


Figure 10-5. Signals $\frac{3\pi}{2}$, or 270°, out of phase

Figure 10-5 shows a phase shift of $3\pi/2$ radians (270°). Notice that the output frequency and the duty factor has decreased to 50%; once again producing an average output voltage of ½$V+$.

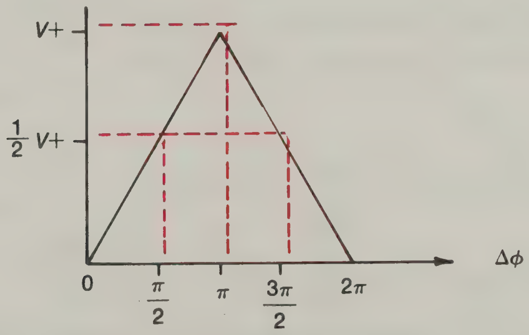


Figure 10-6. $\Delta\phi$ vs. V_{ave} characteristic curve of ex-OR phase detector

The output characteristics of an ex-OR phase detector is represented graphically in **Figure 10-6.** It can be seen that the phase detector output voltage increases linearly, as the phase difference increases form zero to π radians. As the phase difference increases from radians to 2 π radians, the output voltage declines to zero.

Determining the phase difference of two out-of-phase digital signals is quite simple. See **Figure 10-7.**

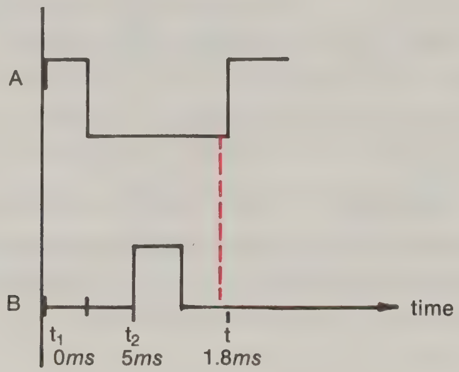


Figure 10-7. Phase difference of two out-of-phase digital signals

From the formula given for phase difference:

$$\Delta\phi = \frac{t_2 - t_1}{T} \tag{10-4}$$

$$\Delta\phi = \frac{5\ msec - 0\ msec}{1.8\ msec} \times 2\pi$$

$$\Delta\phi = 17.44 \text{ radians}$$

There are several digital logic exclusive-OR gates, such as the 7486 TTL IC and the 4030 or 74C86 CMOS gates. An exclusive-OR gate can also be implemented with a Norton amplifier comparator, as shown in **Figure 10-8.**

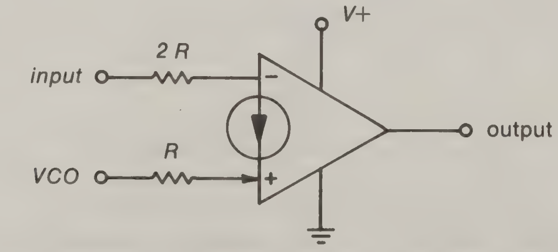
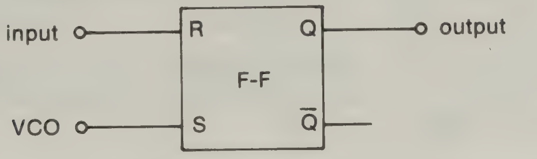


Figure 10-8. Norton amplifier phase detector

Edge-triggered flip-flops are also used as digital phase detectors. They offer several advantages over the exclusive-OR type phase detector. Edge-triggered phase detectors do not require input signals with 50% duty factors. They also offer better capture, tracking, and locking characteristics than the ex-OR type. The draw-back of this type of detector is that both inputs must never be high at the same time. **Figure 10-9** shows an RS flip-flop, used as an edge-triggered phase detector, and the flip-flop's truth table.



R	S	Q	$\bar{Q}$
0	1	1	0
1	0	0	1
0	0	MEMORY	
1	1	AMBIGUOUS	

Figure 10-9. RS flip-flop edge-triggered phase detector

If both inputs go low, the outputs will remain in whatever state they were in before the inputs went low (memory state). The *Q* output is the output of the phase detector. If the S input goes high, the *Q* output will also go high (set state). If the R input goes high, the *Q* output will go low (reset state). Both inputs of the RS flip-flop cannot be allowed to be high at the same time, since this creates an ambiguous output state. For this reason, the RS flip-flop works best as an edge-triggered phase detector, when input pulses are very short in duration.

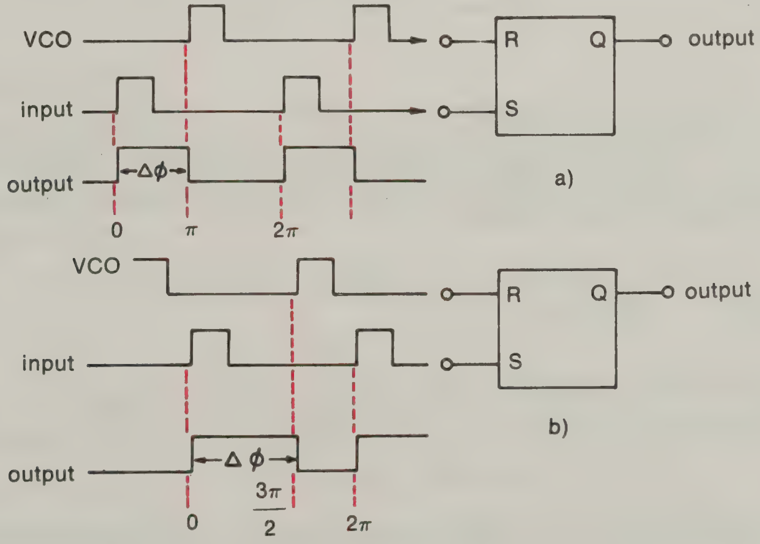


Figure 10-10. Operation of RS flip-flop phase detector

The operation of the RS flip-flop is illustrated in **Figure 10-10.** The output of the flip-flop is triggered on the positive going edge of the input pulses. In part "a" of the figure, the output goes high on the leading edge of the incoming pulse. The output remains high after the trailing edge goes through, because the flip-flop goes into its memory state. When the leading edge of the feedback signal is introduced to the R input, the output goes low (at π). The duty factor of the output is 50%, giving an average output voltage equal to ½ $V+$ for π radians (180°) phase difference.

In part "b" of the figure, the phase difference has been increased to $3\pi/2$ radians. It can be seen that the output remains high much longer than in part "a". The average output voltage has been increased to ¾ $V+$. The output voltage will continue to increase toward $V+$, as the phase difference increases to 2π. If the inputs are allowed to be high at the same instance of time, the flip-flop will be in an ambiguous state and the detector will not function properly. The RS phase detector produces the output characteristic curve shown in **Figure 10-11.**

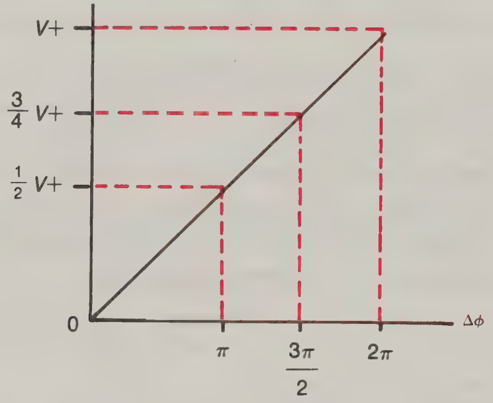


Figure 10-11. $\Delta\phi$ vs. V_{ave} characteristic curve of RS flip-flop

The output of the edge-triggered phase detector is linear over the entire range of phase difference, while the ex-OR type detector will have the same output voltage for two different values of phase difference.

Topic Review 10-2

1. The function of the phase detector is to produce an average DC ______ ______ that is proportional to the ______ difference between the input and feedback signals.

2. Phase difference is the ______ between two related events, expressed in ______ or ______

3. Phase detectors are either the ______ or ______ type.

4. Two types of digital phase detectors are the ______-______ , and the ______-______ flip-flop.

5. Edge-triggered phase detectors offer better ______ , ______ , and ______ characteristics than the ex-OR type.

6. The output of the ______ - ______ phase detector is linear over the entire range of phase difference.

7. The ______-______ phase detector will have the same output voltage for two different values of phase difference.

Answers:

1. error voltage, phase
2. time, degrees, radians
3. analog, digital
4. exclusive-OR, edge-triggered
5. capture, tracking, locking
6. edge-triggered
7. ex-OR

10-3 Double-Balanced Mixer

A double-balanced mixer is used as the phase detector in analog PLL circuits. The circuit is simply a four-diode configuration which mixes the VCO and input signals to produce sum and difference signals. A simple double-balanced mixer is shown in **Figure 10-12.**

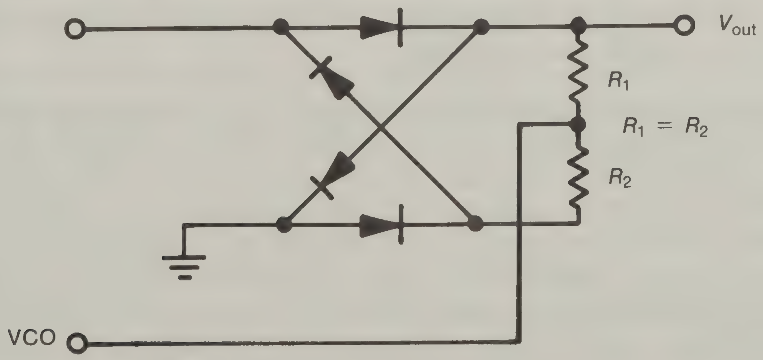


Figure 10-12. A double-balanced mixer

The analog phase detector produces a somewhat different output response than the digital phase detectors discussed so far. **Figure 10-13** shows a typical phase difference response curve for a double-balanced mixer.

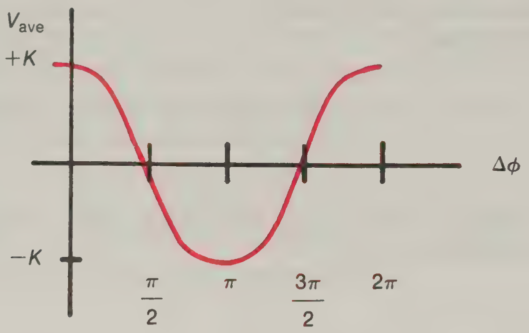


Figure 10-13. Phase response of a double-balanced mixer

The output response is not linear as it was with the digital detector. It's a cosine function, alternating between a maximum positive and negative voltage (±K). The value of K is determined by the input voltage level, the feedback voltage level, and the voltage gain of the stage. The phase detector's output voltage is maximum when the two signals are in-phase. The output decreases through zero at 90° phase difference, $(\frac{\pi}{2})$, and reaches a maximum negative value when the phase difference is 180° (π radians).

Topic Review 10-3

1. A ______-______ ______ is used as the phase detector in analog PLL circuits.
2. The circuit is a four-diode configuration which mixes the VCO and input signals to produce ______ and ______ signals.
3. The double-balanced mixer's output voltage is ______ when the two signals are in-phase.

Answers:

1. double-balanced mixer
2. sum, difference
3. maximum

10-4 Low-Pass Filter (Integrator)

The loop filter is the most important part of the PLL system. The filter stage controls the lock range, capture range, bandwidth, and transient response of the loop. It receives the error signal from the phase detector and produces an average DC voltage to drive the VCO stage.

An in-depth explanation of the loop filter becomes very mathematical in nature and is beyond the scope of this text. However, there are some terms and general equations that should be covered in any explanation of phase-locked loops.

The frequency at which the loop will oscillate (in the absence of damping or offset components) when a transient occurs is the loop's *natural frequency* (ω_n). The loops undamped natural frequency is usually equal to the center or design frequency of the circuit, and is determined by the loop filter's cutoff frequency (ω_r) and DC loop gain. DC loop gain is simply the combined gains of the detector (K_D) and the VCO (K_O). For a simple, passive, low-pass filter the undamped natural frequency can be calculated by:

$$\omega_r = \frac{1}{RC} \tag{10-5}$$

$$\omega_n = \frac{1}{(K_O K_D \omega_r)} 2 \tag{10-6}$$

The filter also determines the loop's *transient response*, or the manner in which the loop will respond to changes in input frequency. This is dependent on the damping of the filter. **Damping is the ability of the loop to respond quickly to changes in input frequency without excessive overshoot.** The filter's *damping factor* (α) is the ratio of its overshoot voltage to its settling time, and can be calculated by:

$$\alpha = \frac{1}{2}\left(\frac{\omega_r}{K_O K_D}\right)^{1/2} \tag{10-7}$$

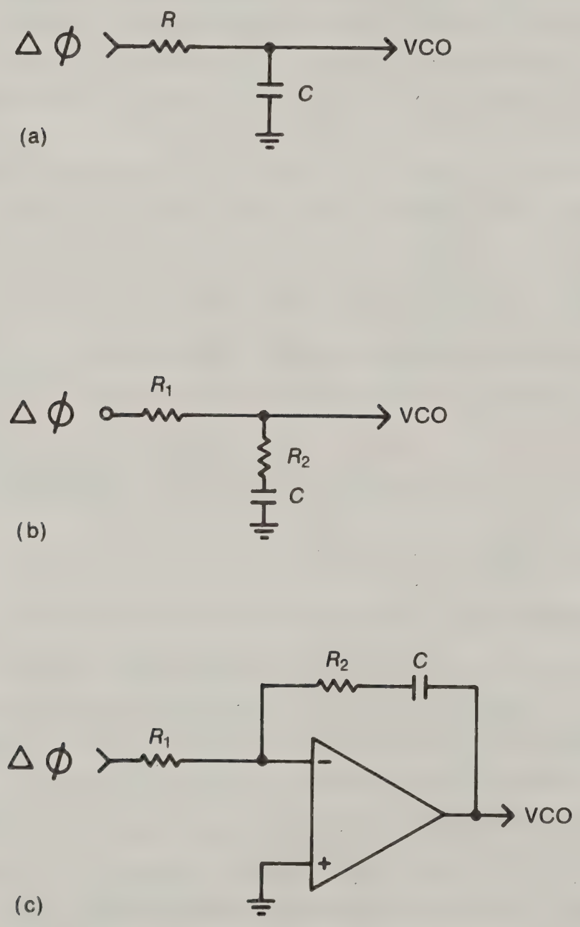
for the first-order *RC* low-pass filter.

Damping factors are normally established between 0.5 and 0.8. Higher damping factors tend to cause the PLL to react too slowly when trying to lock onto an incoming frequency. Smaller damping factors will cause the loop to try to lock onto frequencies outside the capture range. The frequency at which the loop will oscillate, when a transient occurs in the presence of damping (or offset), is called the loop's damped natural frequency. This frequency is the same as the offset center frequency.

Overshoot occurs when the input frequency changes, because the filter cannot respond instantly to the change. As the filter output moves toward the new value, the output will tend to overshoot the new value, swing above and below the new frequency for a short time, and eventually settle down to the new value. **The time required**

for the loop to respond to a change in input, and settle within 10 percent of the new value, is termed *settling time.*

There are other types of low-pass filters which are used with PLL's. Three of these are shown in **Figure 10-14.** Part "a" of the figure shows a typical passive, first-order low-pass filter, with its associated formulas. Part "b" of the figure depicts a first-order, lead-lag, low-pass filter and its formulas. This filter is especially well suited to the exclusive-OR type phase detector, where a given value of average voltage has two meanings, depending on the lead-lag relationship of the input signals. Part "c" shows an active low-pass filter and its equations.



(a)

$$\omega_r = \frac{1}{RC} \text{ (rads/sec)}$$

$$\omega_n = (K_c K_o \omega_r)^{1/2}$$

$$\alpha = \frac{1}{2}\left(\frac{\omega_r}{K_o K_c}\right)^{1/2}$$

(b)

$$\omega_r = \frac{1}{(R_1 + R_2)\,C}$$

$$\omega_n = (K_c K_o \omega_r)^{1/2}$$

$$\alpha = \frac{\omega_n}{2}\left[\, R_2 C + \left(\frac{1}{K_o K_c}\right)\right]$$

(c)

$$\omega_r = \frac{1}{R_1 C}$$

$$\omega_n = (K_c K_o \omega_r)^{1/2}$$

$$\omega = \left(\frac{R_2 C}{2}\right)\omega_n$$

Figure 10-14. Low-pass loop filters

For a PLL to acquire a lock condition, the filter must produce a surge of error voltage to initiate the locking process. This surge is called a *transient* and its amplitude is determined by the damping factor of the filter. Only a certain band of frequencies will cause a change in the filter's output voltage. This band of frequencies represents the active bandwidth of the filter, and frequencies outside of the bandwidth have no effect on the filter's response voltage.

The range of frequencies over which the loop can obtain phase-lock is called the *capture range* or ω_c. The capture range extends equally above and below the free-running frequency of the VCO, and is determined by the formula:

$$\omega_c = 4\alpha\omega_n \tag{10-8}$$

From this equation we can see that the capture range of the loop is determined primarily by the characteristics of the loop filter.

On the other hand, the range of frequencies over which the loop will track changes in input frequency, or *lock range*, (ω_l), is determined solely by the DC loop gain.

$$\omega_l = 2\,K_D\,K_O \text{ in Radians/Second} \tag{10-9}$$

Topic Review 10-4

1. The filter stage controls the ______ range, ______ range, ______ and ______ ______ of the loop.

2. The filter receives the error signal from the phase detector and produces an ______ ______ ______ to drive the VCO stage.

3. The undamped frequency at which the loop will oscillate when a transient occurs is the loop's ______ ______.

4. The transient-response is the manner in which the loop will respond to changes in ______ ______.

5. ______ is the ability of the loop to respond quickly to changes in input frequency without excessive overshoot.

6. The filter's damping factor is the ratio of its ______ voltage to its settling time.

7. The time required for the loop to respond to a change in input, and settle within 10 percent of the new value, is termed ______ ______

Answers:

1. lock, capture, bandwidth, transient response
2. average DC voltage
3. natural frequency
4. input frequency
5. Damping
6. overshoot
7. settling time

10-5 Voltage-Controlled Oscillator

The function of the VCO stage is to convert the output voltage of the filter stage into a frequency signal, which is fed back to the phase detector stage. The output frequency of the VCO is directly proportional to its input voltage. The characteristics of the VCO stage can be expressed as:

$$\omega_O = K_O V_F \text{ (in Radians/Sec)/Volt} \qquad (10\text{-}10)$$

where: ω_O = VCO Output Frequency in Radians/Second
K_O = VCO Conversion Gain (Constant)
V_F = Input Voltage From the Filter Stage

There are several types of VCOs that may be used in a phase-locked loop system. The discrete VCO described in Chapter 7 may be used. Also, several IC VCOs are available: the MC4024 and MC1648, the XR2206 function generator and the 566 VCO.

A VCO can be implemented by replacing the standard capacitor in a tank circuit with a varactor diode. The varactor simply utilizes the capacitive properties of a diode junction, to produce a voltage-variable capacitor. The schematic symbol for a varactor diode and its mechanical representation are shown in **Figure 10-15.**

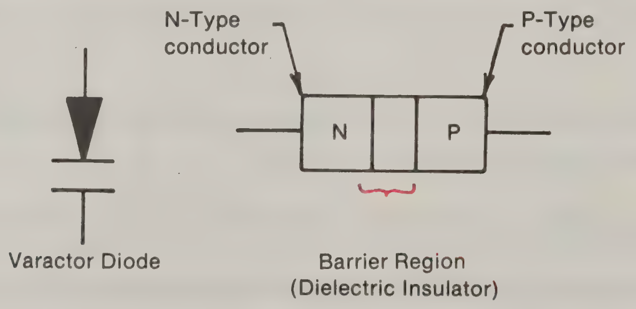


Figure 10-15. Varactor diode action

The barrier region of a diode acts as a dielectric between an *N*-type and a *P*-type conductor. This is the definition of a capacitor. Since the barrier region can be increased or decreased by increasing or decreasing the voltage across the diode, the diode can be used as a voltage variable capacitor. The varactor may be used in either series resonant or parallel resonant configurations.

Topic Review 10-5

1. The function of the VCO stage is to convert the ______ ______ of the loop filter into a ______ ______.

2. The output frequency of the VCO is usually ______ ______ to its input voltage.

3. A VCO can be implemented by replacing a standard capacitor in a tank circuit with a ______ ______.

4. The varactor simply utilizes the ______ properties of a diode junction.

Answers:

1. output voltage, frequency signal
2. directly proportional
3. varactor diode
4. capacitive

10-6 566 VCO

The 566 is a single package, general purpose VCO, which requires few external components. This monolithic VCO requires only an external timing resistor and capacitor to produce both square and triangular output waveforms. An internal diagram of the 566 is shown in **Figure 10-16.**

Upon close inspection, we can see that the 566 operates in much the same manner as the discrete VCO, constructed with Norton amplifiers in Chapter 7. The 566 replaces the Norton integrator with a pair of matched constant current sources. The constant current sources cause the timing capacitor to charge and discharge in a linear fashion.

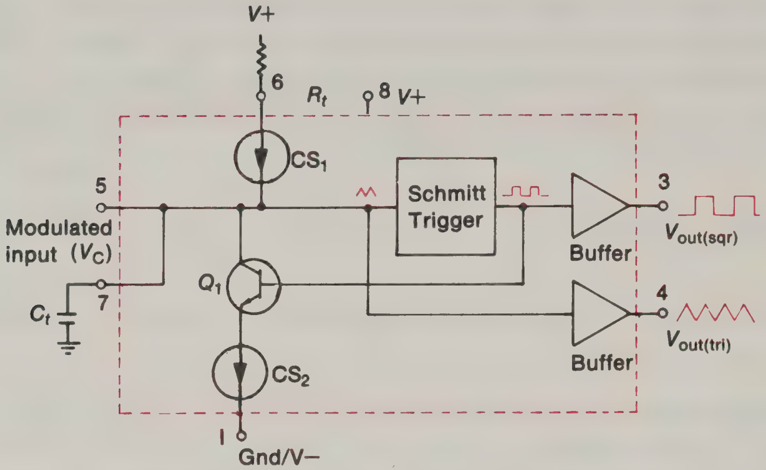


Figure 10-16. Internal diagram of the 566 VCO

The amount of current delivered by the constant current source is controlled by both an external timing resistor (R_t), and the value of the modulating input or control voltage (V_C). In this configuration, the value of current delivered to the Schmitt trigger and C_t is inversely affected by the value of V_C. As V_C increases, the current delivered to the timing capacitor and the Schmitt trigger decreases, causing the output frequency to also decrease. When the 566 is first powered up, there is no charge on the timing capacitor and the output of the Schmitt trigger is forced low, turning off control transistor (Q_1). The capacitor charges linearly through CS1 until it reaches the upper trip point (utp) voltage of the Schmitt trigger. At this point the output of the Schmitt trigger goes high and turns Q_1 on. This causes the capacitor to discharge linearly through CS2 until it reaches the lower trip point (ltp) voltage of the Schmitt trigger and the cycle begins again.

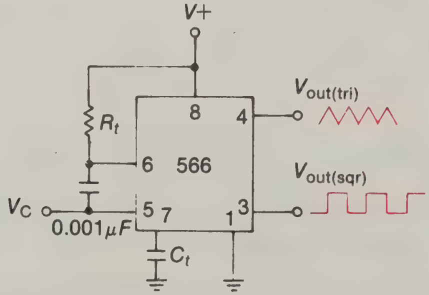


Figure 10-17. A typical 566 VCO without offset

In the functional diagram of **Figure 10-17** the full output frequency range of the 566 is available. A small frequency compensating capacitor (0.001μF) is inserted between pins 5 and 6. The maximum output frequency is determined by:

$$f_{out(max)} = \frac{2(V+) - \omega_{c(max)}}{R_t\, C_t\, (V+)} \tag{10-11}$$

The value of R_t should be between 2 *k*ohms and 20 *k*ohms which allows a 10-to-1 frequency adjustment range. The VCO's output frequency can be offset by introducing a permanent offset at the modulation input. This offset may be introduced through a resistive voltage divider, as shown in **Figure 10-18**

The input control voltage V_C is added to the offset voltage produced by the resistive voltage divider. The offset voltage must be greater than $\frac{3}{4}$ of V+, but less than V+. Values of R_1 and R_2 should be chosen between 1 *k*Ω and 100 *k*Ω.

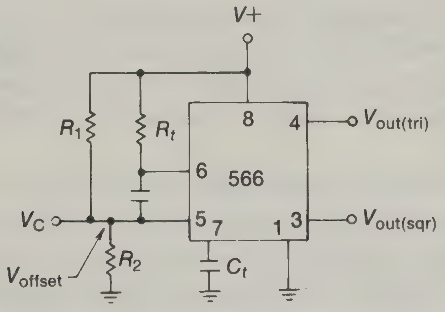

V+
R1
Rt
8
4
Vout(tri)
6
566
VC
5
7
1
3
Vout(sqr)
R2
Ct
Voffset

Figure 10-18. The 566 VCO with input offset

10-7 Norton Amplifier PLL

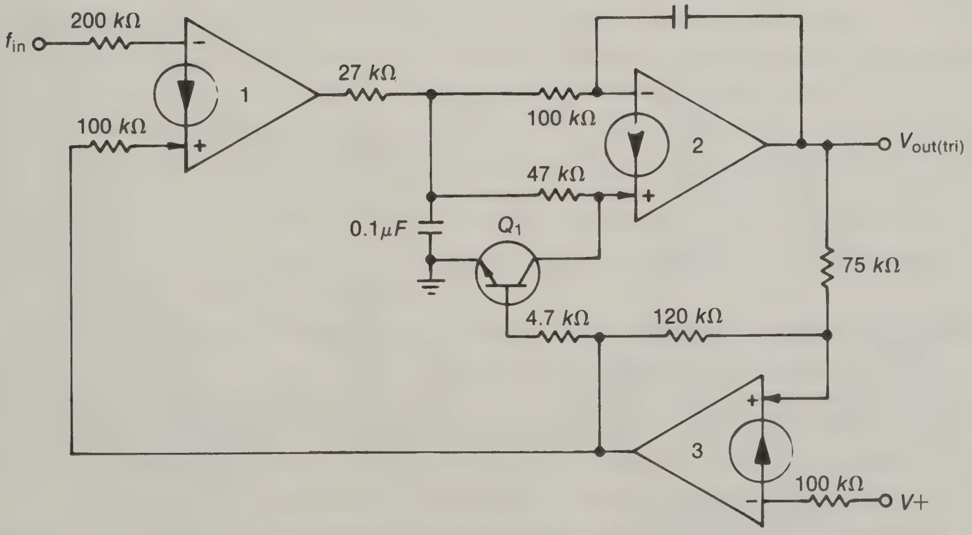

fin
200 kΩ
−
+
1
100 kΩ
27 kΩ
100 kΩ
47 kΩ
2
Vout(tri)
0.1µF
Q1
75 kΩ
4.7 kΩ
120 kΩ
3
100 kΩ
V+

Figure 10-19. Norton amplifier PLL

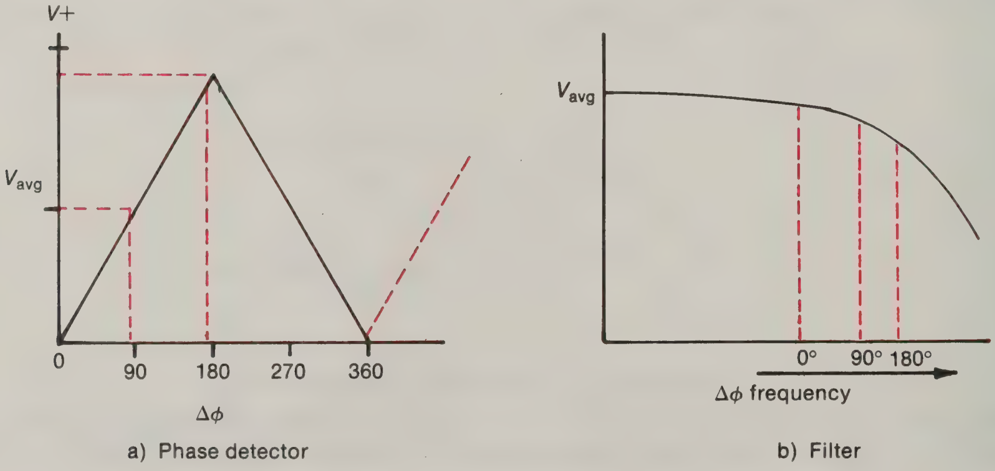
A PLL circuit, constructed on a single Norton amplifier chip, is shown in **Figure 10-19.** Amplifier number 1 is configured as an ex-OR phase detector. Amplifiers 2 and 3 are used to form the VCO. The passive loop filter consists of the 27 *k*ohm resistor and the 0.1 μF capacitor.

The phase detector produces the phase difference response discussed earlier. When no input signal is present, only the VCO feedback signal is applied to the phase detector, to be converted into an error voltage. In this condition, the ex-OR phase detector produces a 50% duty factor, which corresponds to a 90° phase difference and an average DC error voltage of one-half of *V*+. The exclusive-OR phase detector is prone to lock into harmonics of the VCO center frequency.

The filter acts as an integrator which controls the loop's capture frequency and capture range, or bandwidth. To a lesser extent, the filter controls the loop's lock frequency and lock range. Only frequencies within the bandwidth of the detector/filter combination will affect its output. Frequencies outside the filter's bandwidth won't affect its output.

The filter's output voltage is applied to the VCO stage which converts the input voltage to a directly proportional output frequency. The VCO frequency range is the major determining factor in the loop's lock or tracking range. Basically, there are four ways of adjusting this VCO's frequency: 1) decreasing the value of the integrator's feedback capacitor will increase the output frequency range, 2) decreasing the value of the integrator's input resistors will increase the frequency range, 3) bringing the utp and ltp of the Schmitt trigger closer together will increase the output frequency, and 4) increasing the VCO's input voltage will increase its output frequency.

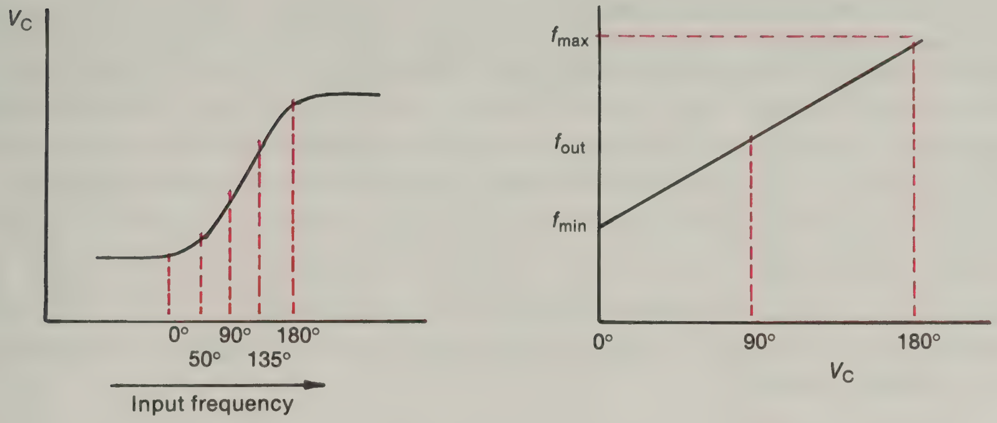
Figure 10-20 shows the response characteristics of the individual stages of the loop.



a) Phase detector

b) Filter

Figure 10-20. Response characteristics of PLL stages



c) Error voltage

d) VCO

Figure 10-20. (continued)

When no input frequency is applied to the PLL, only the feedback VCO frequency will be processed through the loop filter and converted into a DC error voltage. The VCO frequency alone, causes the phase detector to produce a fifty-percent duty cycle output. This corresponds to a 90° phase difference, causing the VCO to produce its designed center frequency.

If an input frequency is introduced, which is well below the loop's lower lock frequency, the phase comparator produces an output which is a combination of the input and VCO frequencies. Since the input frequency is not within the detector/filter bandwidth, only the VCO component is converted into error voltage.

As the input frequency increases, a point will be reached where it is close enough to the VCO frequency to cause the error voltage to decrease from its 90° center frequency position. This point is the loop's lower capture frequency, f_{cl}. The decrease in error voltage will cause the VCO output frequency to decrease until it is equal to the input frequency with a phase shift of approximately 50°. If the input frequency continues to increase, so will the output frequency with only an increase in the phase shift between the two. Likewise, a decrease in input frequency will cause the VCO frequency and phase shift to decrease.

Once lock has been obtained, the loop will be able to track the input frequency up to approximately 179° or down to 0°. These points represent the upper and lower lock frequencies. Once the phase difference exceeds these points, the phase detector's output frequency is outside the bandwidth of the filter and only the VCO signal will produce an error voltage. This causes the VCO to return to its center frequency. A higher input frequency descending toward the center frequency will reach a point called the upper capture frequency (f_{cu}) causing the error voltage to increase until lock occurs.

10-8 The Integrated Circuit PLL

The phase-locked loop circuits discussed up to this point have been assembled with discrete components. As with so many other applications today, most of the circuit elements can be replaced by a single IC. These IC packages contain the phase detector and VCO. Most often, other circuitry is included to meet various special requirements. External to the package, are the few components which make up the loop filter. These IC PLLs may contain either a digital or analog phase detector.

The 4046 is a digital phase-locked loop IC which contains both an ex-OR and an edge-triggered phase detector and an on board VCO. A source follower is also included to allow the DC error voltage to be used without loading the signal. An undedicated zener diode is provided for use as a regulated supply voltage. The VCO can be disabled by an external inhibit signal (pin 5). A block diagram of the 4046 is shown in **Figure 10-21.**.

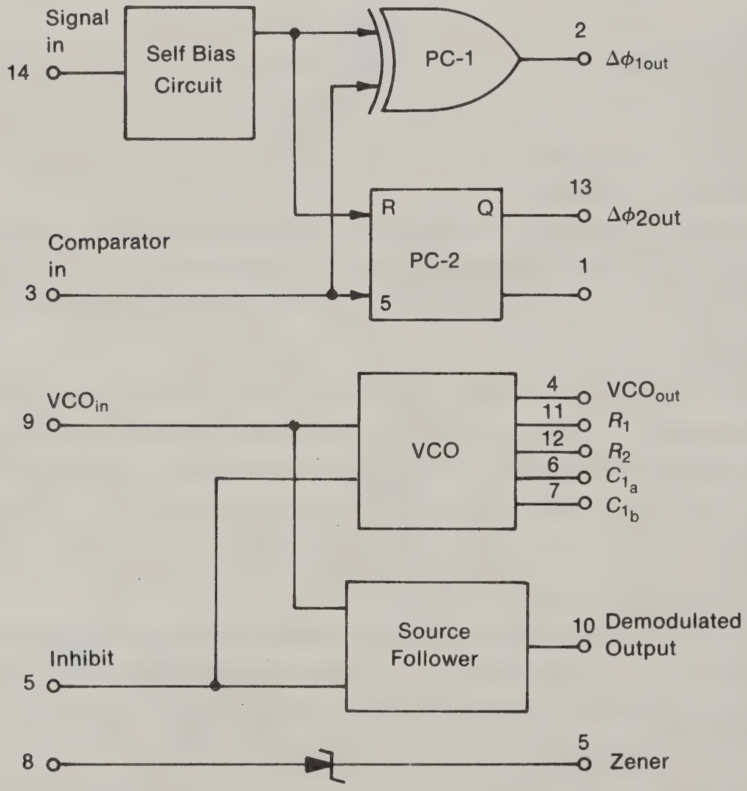

Signal in
14
Self Bias Circuit
PC-1
2
Δϕ1out
R
Q
13
Δϕ2out
Comparator in
3
PC-2
5
1
VCO_in
9
VCO
4
VCO_out
11
R1
12
R2
6
C1a
7
C1b
Source Follower
10
Demodulated Output
Inhibit
5
8
5
Zener

Figure 10-21. Block diagram of 4046 PLL

The only external components necessary are the loop filter (usually a lead-lag type with a variable resistance to allow the filter to be adjusted for desired loop characteristics) and 3 VCO frequency determining components C_1, R_1, and R_2. A typical 4046 PLL configuration using the exclusive-OR phase detector is shown in **Figure 10-22.**

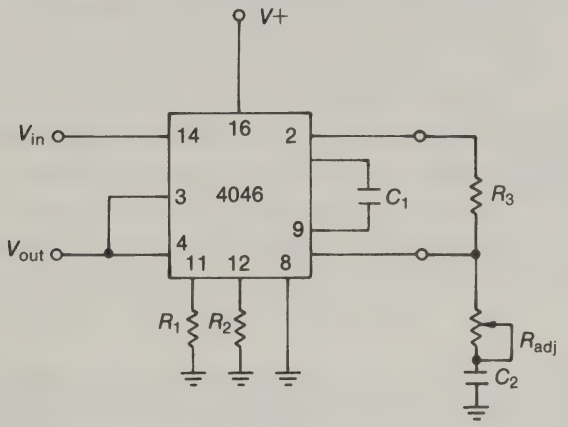


Figure 10-22. A typical 4046 PLL configuration

The manufacturer's data sheets provide design procedures and formulas for the 4046. Component values are chosen from graphs found in the data sheets. The VCO frequency is set by R_1 and C_1 while its minimum output frequency is determined by the relationship of R_2 to C_1. If no minimum frequency offset is desired, the R_2 terminal may be left open and the minimum VCO output frequency will be near 0 *Hz*. Values of R_1 and R_2 should be chosen between 10 *kΩ* and 1 *MΩ*. C_1 should be greater than 100 *pF*.

The loop's lock range is determined by the VCO's frequency relationships and its capture range is set by the loop filter. Formulas for both relationships are found in the data sheet.

An important point to bring up here is that each series of integrated circuits (i.e., 4046, 565, etc.) has design formulas which are uniquely their own. These formulas are found on the manufacturer's data sheet. Also, it is interesting to note that frequency is stated in *Hz* rather than the radians/second used for discrete PLL circuit analysis.

Topic Review 10-8

1. The 4046 is a digital phase-locked loop IC which contains both an ______-______ and an ______-______ phase detector and an on board ______.

2. The only external elements necessary with the 4046, are the ______ ______, and VCO ______ determining components.

3. Each series of integrated circuit PLL has ______ ______ which are uniquely their own.

4. The formulas are found on the manufacturer's ______ ______.

Answers:

1. ex-OR, edge-triggered, VCO
2. loop filter, frequency
3. design formulas
4. data sheet

10-9 LM565 PLL

One of the most popular IC phase-locked loops available is the 565 PLL. The 565 is a general purpose, analog phase-locked loop which contains a double-balanced phase detector and a VCO very similar to the 566 discussed in this chapter. This is an inverting VCO. When the VCO input voltage increases, the output frequency decreases and when the input voltage decreases, the output frequency increases. The 565 provides two signal input terminals which drive a differential amplifier to allow the use of a differential input signal. A block diagram of the 565 is shown in **Figure 10-23.**

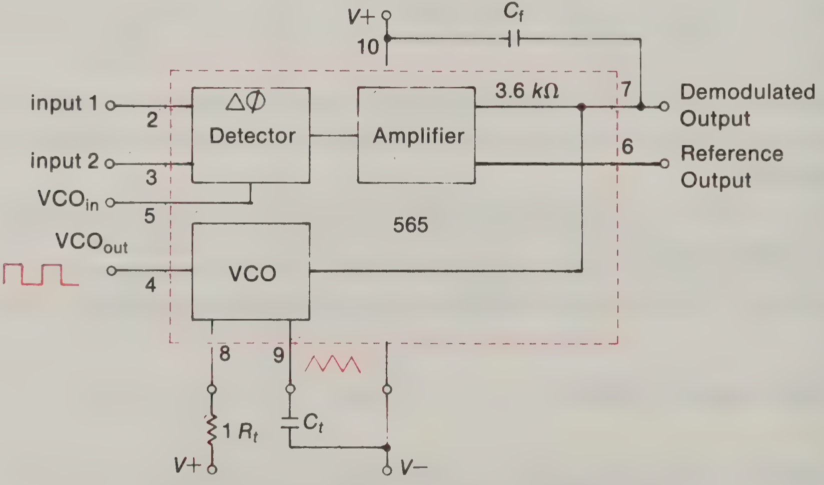
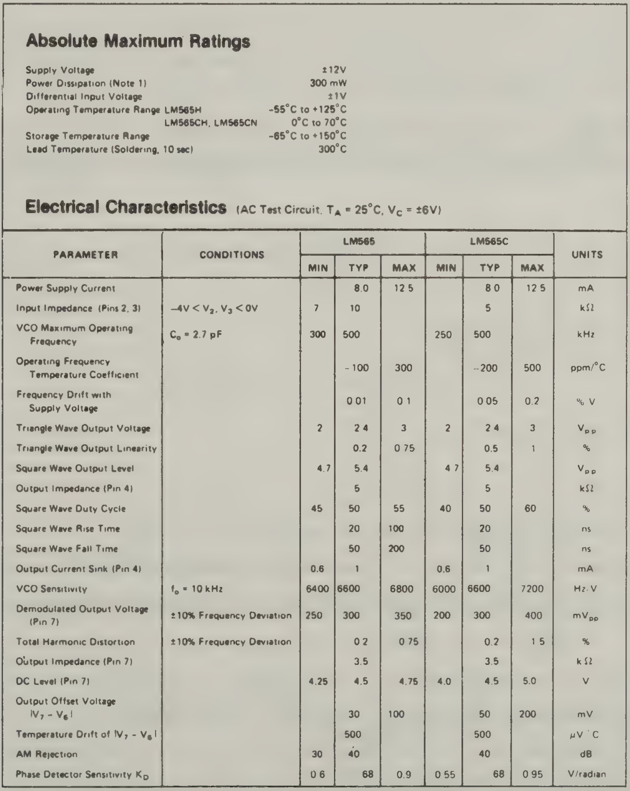

V+
10
C_f
input 1
2
input 2
3
VCO_{in}
5
VCO_{out}
4
ΔΦ
Detector
Amplifier
3.6 kΩ
7
6
Demodulated Output
Reference Output
565
VCO
8
9
1 R_t
C_t
V+
V−

Figure 10-23. Block diagram of 565 PLL

The 565 comes in both 10-pin metal cannister and 14 pin DIP packages. Pins 10 and 1 are the chip's positive and negative supplies respectively. Pins 2 and 3 are the inputs of the differential amplifier which drive the phase detector. If a differential input is not used, the input signal is applied to one of the pins with the other pin grounded. Pins 4 and 5 form the loop's feedback path. These pins allow for the insertion of divider networks used in some applications. Normally, these two pins will be tied together and the loop's output is taken from pin 4. The demodulated output (pin 7) simplifies the loop's filter design. An internal 3.6 *k*Ω resistor allows the user to simply choose an appropriate value of capacitance (C_f) to complete the loop filter. C_f is connected between the output and the positive supply voltage. This output allows the error voltage and demodulated signal from frequency changes to be sampled and used. The reference output (pin 6) can be used to change the loop's lock range by connecting a resistor between this output and pin 7. Normally, this pin is left open. Pins 8 and 9 allow the user to control the center frequency of the VCO with a timing resistor (R_t) and capacitor (C_t). A triangular output waveform is available at pin 9. In the 14-pin DIP, pins 11 through 14 are not used.



Absolute Maximum Ratings

Supply Voltage	±12V
Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±1V
Operating Temperature Range LM565H	−55°C to +125°C
LM565CH, LM565CN	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (AC Test Circuit, $T_A = 25°C$, $V_C = \pm 6V$)

PARAMETER	CONDITIONS	LM565			LM565C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	$C_o = 2.7$ pF	300	500		250	500		kHz
Operating Frequency Temperature Coefficient			−100	300		−200	500	ppm/°C
Frequency Drift with Supply Voltage			0.01	0.1		0.05	0.2	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{pp}
Triangle Wave Output Linearity			0.2	0.75		0.5	1	%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{pp}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20	100		20		ns
Square Wave Fall Time			50	200		50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	$f_o = 10$ kHz	6400	6600	6800	6000	6600	7200	Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	350	200	300	400	mV_{pp}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\|V_7 - V_6\|$			30	100		50	200	mV
Temperature Drift of $\|V_7 - V_6\|$			500			500		μV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D		0.6	68	0.9	0.55	68	0.95	V/radian

Figure 10-24. Data sheet, Courtesy National Semiconductor Corp.

Referring to the manufacturer's data sheets in **Figure 10-24,** there are some important points. The 565 requires a split supply voltage between ±6 *V* and ±12 *V*. The device also requires a minimum input signal amplitude of 10*mV* rms for tracking with a maximum allowable input level of 3 *Vp-p*. The 565 produces two output waveforms: a TTL compatible square wave (pin 4, using +6 *V* supply) and a triangle wave (pin 9); each with a frequency range from 0.001 *Hz* to 500 *kHz*, and a phase lock bandwidth, adjustable from less than 1% to greater than 60% of the center frequency. Using a +6 volt supply, the loop produces 5.4 *Vp-p* square waves and extremely linear 2.4 *Vp-p* triangle waves.

The first step in designing a PLL using the 565 is to establish the free-running frequency of the loop. This is actually the center frequency of the VCO which is calculated from the fromula:

$$f_r = \frac{1}{3.7\, R_t\, C_t} \tag{10-12}$$

where: $R_t = 2\ k\Omega$ to $20\ k\Omega$

The center frequency (f_r) is inversely proportional to both R_t and C_t. Increasing the value of either component will cause the center frequency to decrease and vice-versa.

Due to the inherent characteristics of the 565, the loop's lock range varies inversely to the IC's voltage. If supply voltage is increased, the lock range decreases and conversely, a decrease in supply voltage increases the lock range. The lock range can be calculated by:

$$f_{\mathrm{LR}} = \frac{8\, f_r}{V_{\mathrm{R}}} \tag{10-13}$$

and minimum lock frequency by:

$$f_{\mathrm{Lmin}} = f_r - f_{\mathrm{LR}} \tag{10-14}$$

and maximum lock frequency by:

$$f_{\mathrm{Lmax}} = f_r + f_{\mathrm{LR}} \tag{10-15}$$

where the supply voltage range (V_{R}) is equal to $V+ - (V-)$.

The capture range of the loop is primarily determined by the loop filter. Since the 565 IC provides a fixed 3.6 $k\Omega$ internal resistor the capture range is dependent largely on the value of C_f.

$$f_c = \pm \left[\frac{f_{\mathrm{LR}}}{2\pi(3.6k)(C_f)} \right]^{1/2} \text{ (in } Hz\text{)} \tag{10-16}$$

The larger the value of C_f, the smaller the lock and capture ranges will be.

A standard 565 PLL configuration is shown in **Figure 10-25.**

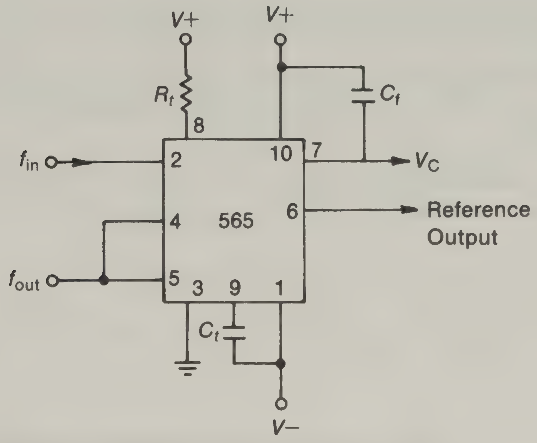


Figure 10-25. Basic 565 PLL configuration

A variable lock range PLL can be constructed by placing a 1 $k\Omega$ resistor and a 0-1 $M\Omega$ variable resistance in series between pins 6 and 7.

Topic Review 10-9

1. The 565 is a general purpose analog PLL, which contains a ______-______ ______ phase detector.

2. Due to the inherent characteristics of the 565, the loop's lock range varies ______ to the IC's supply voltage.

Answers:

1. double-balanced mixer
2. inversely

10-10 Frequency Multiplication

A PLL can be used to multiply a basic input frequency by placing a frequency divider in the VCO feedback loop as shown in **Figure 10-26.**

The basic digital frequency divider is the master-slave, toggle flip-flop. The output of this device changes from one logic state to the other (high to low or low to high) when a complete square wave is applied to it. On the rising edge of the square wave the change is loaded onto the master part of the flip-flop. On the falling edge, the output is processed through the slave section and appears at the output of the

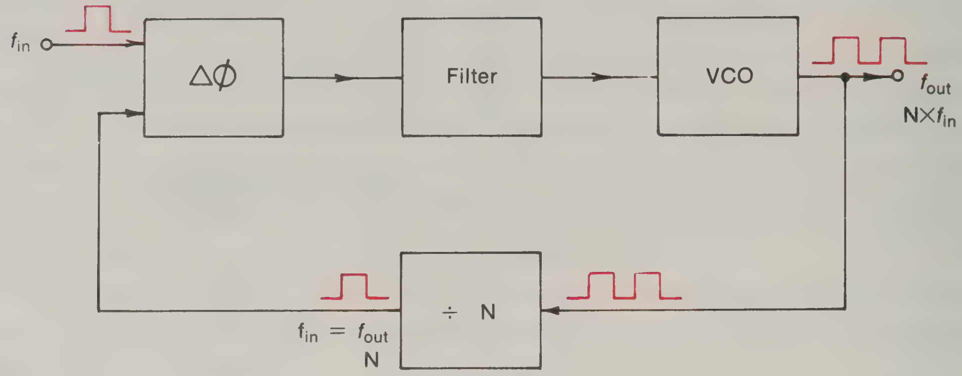


Figure 10-26. PLL frequency multiplier

flip-flop. The flip-flop requires two complete changes of input logic levels to produce one change of output logic level. In effect the flip-flop will divide the input frequency by two. Cascaded flip-flops in the feedback loop can be used to divide by 4, 8, 16, 32, etc. These basic dividers can be decoded to any count level desired. IC manufacturers produce a number of digital counter chips which can be used as frequency dividers. The 74190 MOD-10 counter is an example of an IC which can be used as a divide by 10 device.

The frequency multiplication operation is quite simple. If the PLL is in the lock mode, the two input frequencies must be equal. Since the VCO feedback signal is being divided by "N," the VCO output frequency must be "N" times greater than the phase detector input frequency.

This operation is limited only by the maximum output frequency of the VCO. If a programable "N" counter is used, a number of frequencies can be generated with the same circuit. This practice is known as frequency synthesis. The divide-by-counter is programed with binary code, from a set of external switches, which determines the maximum count (N) of the device. Each time the code is changed, the PLL will cause the VCO to generate an output frequency that is "N" times the basic input frequency. Frequency synthesizers can be found in many applications, such as transceivers, touch-tune television tuners, electronic organs, and so forth.

Topic Review 10-10

1. A PLL can be used to multiply a basic input frequency by placing a ________ ________ in the VCO feedback loop.

2. Since the VCO feedback signal is being divided by "N", the VCO output frequency

must be “N” times ______ ______ the phase detector input frequency.

3. If a programable “N” counter is used, a number of frequencies can be generated with the same circuit. This practice is known as ______ ______.

4. Frequency synthesizers can be found in many applications, such as ______, touch-tune ______ ______, electronic ______ and so forth.

Answers:

1. frequency divider
2. greater than
3. frequency synthesis
4. transceivers, television tuners, organs

0-11 Summary Points

1. A phase-locked loop is a feedback loop system which can lock onto an input frequency signal and track it if it varies.

2. A basic PLL system contains a phase difference detector, a low pass filter, and a VCO.

3. Phase difference is the time between the occurrance of two related events such as the rising edges of two square wave signals.

4. The phase detector stage compares the input frequency signal to the feedback VCO frequency and produces an average DC error voltage which is proportional to the phase difference of the two.

5. Exclusive-OR gates, RS flip-flops and double-balanced mixers are used as phase detectors.

6. RS flip-flops require that both inputs not be allowed to be high at the same time.

7. The output of the double-balanced mixer is maximum at 0° phase difference, zero at 90°, and maximum negative at 180°.

8. Ex-OR gates and RS flip-flops are used as phase detectors in digital applications while double-balanced mixers are used in analog PLLs.

9. The loop filter removes high frequency noise from the circuit, determines the loop's response characteristics, and converts the average error voltage into DC to drive the VCO stage.

10. The loop filter may be passive or active.

11. The VCO converts the DC error voltage into an output frequency signal.

12. PLLs using double-balanced mixers require VCOs which have outputs that are inversely proportional to their input.

13. PLLs have three distinct modes of operation: free running, capture, and lock.

14. In the free running mode, no input signal is near enough to the VCO frequency to be captured. The VCO runs at its center frequency.

15. In the capture mode, an input signal has come close enough to the VCO frequency to cause the output frequency to change.

16. In the lock mode, the output frequency equals the input frequency.

17. Capture range is the range of frequencies over which the loop can acquire lock.

18. Lock range is the range of frequencies over which the loop can track or follow the input signal once lock has been achieved.

19. PLLs are used as frequency multipliers and synthesizers. This is accomplished by placing divide-by N counters in the feedback loop.

10-12 Chapter Progress Evaluation

1. The phase detector stage of the PLL compares which two frequencies?

2. A DC error voltage is generated by the phase detector; this voltages is proportional to what?

3. Which one of the three basic stages of a PLL generates the transient needed to initiate the locking process?

4. What two stages of the loop are commonly contained within the IC packaged PLL?

5. A frequency divider is added to the VCO feedback loop, to convert a PLL into a frequency multiplier. What element is commonly used as a frequency divider and describe briefly how it operates.

6. The programmable frequency divider uses what code for programming and by what means is this code varied.

Chapter 11

Devices and Applications

Objectives

Upon completion of this chapter, you should be able to do the following:

- Describe the internal operation of audio and stereo amplifier ICs and list their uses.
- Describe the operation and applications of voltage-to-frequency converters (V/F) and frequency-to-voltage converters (F/V).
- Describe frequency shift keying (FSK) uses in modern transmitters and receivers.

11-1 Introduction

As a conclusion to this text, we have included a chapter of selected circuits and applications. The first half of the chapter covers a group of National Semiconductor single supply op amps intended for audio applications, such as stereo amplifiers for radios, tape players, recorders, and bass and treble tone control circuits. The second section of the chapter deals with the operation and design of frequency-to-voltage and voltage-to-frequency converters, using the Teledyne 9400 V/F-F/V converter chip. The chapter is concluded with various examples of V/F and F/V converter applications.

11-2 LM377 Dual 2-Watt Audio Amplifier

The National Semiconductor LM377 is a dual op amp package operating with supply voltages between +10 and +26 volts, and can supply 2 watts/channel to an 8 or 16 ohm load. This amplifier offers 75 *dB* of channel separation and a typical open-loop voltage gain of 90 *dB*. Channel separation describes the *ability* of a stereo receiver to produce left and right stereophonic channel signals at its output terminals. These qualities make the LM377 quite useful in such stereo applications as:

stereo receivers, phonographs, tape players, and recorders. In addition, the device contains internal current limiting, thermal overload, and self-center biasing circuitry. By biasing both amplifiers from a common internal regulator, the chip is given a high degree of power supply rejection ratio and precise quiescent output centering.

Figure 11-1 depicts a block diagram of the LM377. The IC consists mostly of a pair of high-performance op amps and an internal biasing circuit. Overload protection circuitry is not shown.

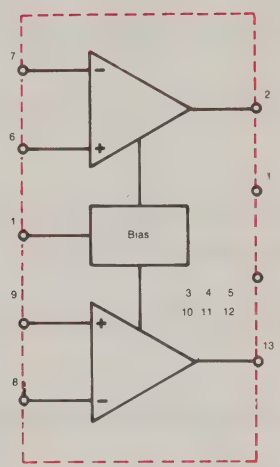


Figure 11-1. LM377 block diagram.
Courtesy of National Semiconductor Corporation

These op amps feature high slew rate, high input impedance (3 $M\Omega$), and internal frequency compensation. The internal regulator is used to set the DC bias level of both op amps in a manner similar to that of the Norton amplifier. (Unlike the Norton, the 377 is a voltage-driven device).

The LM377 can be configured either as inverting or noninverting. The inverting form uses less components, but the noninverting configuration allows the input impedance of the op amp itself to be the input impedance of the circuit.

Figure 11-2 shows the 377 configured in inverting form, and **11-3** shows its noninverting form. Both figures show the 377 configured as a simple stereo output amplifier. DC blocking capacitors are used to filter out any DC component in the audio input signal, and confine the amplifier's DC bias current within the biasing loop. The voltage gain of either configuration can be calculated by the formula:

$$A_v = \frac{R_f}{R_{in}} \qquad \text{(inverting amp)} \qquad (11\text{-}1)$$

or:

$$A_v = \frac{R_f}{R_A} \qquad \text{(noninverting amp)} \qquad (11\text{-}2)$$

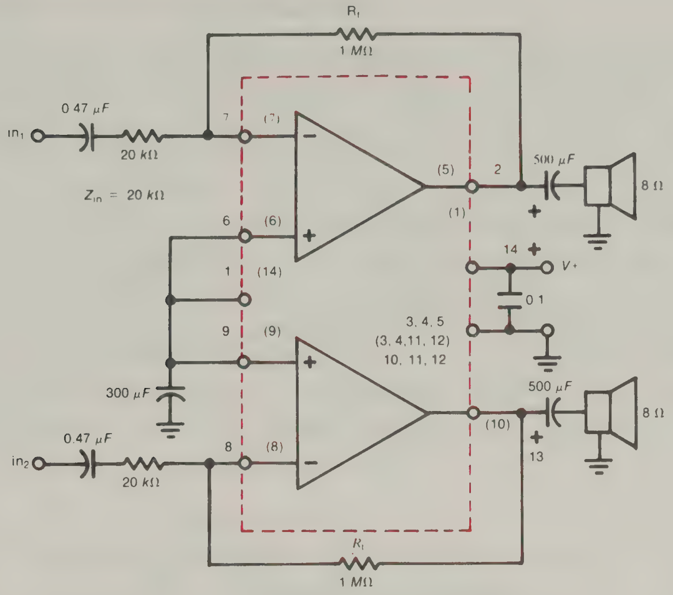

R₁
1 MΩ
0.47 μF
in₁
20 kΩ
Zᵢₙ = 20 kΩ
7
(7)
6
(6)
1
(14)
9
(9)
(5)
2
(1)
500 μF
8 Ω
14
V+
0.1
3, 4, 5
(3, 4, 11, 12)
10, 11, 12
300 μF
500 μF
8 Ω
(10)
13
0.47 μF
in₂
20 kΩ
8
(8)
R₁
1 MΩ

Figure 11-2. LM377 inverting amplifier
Courtesy National Semiconductor Corporation

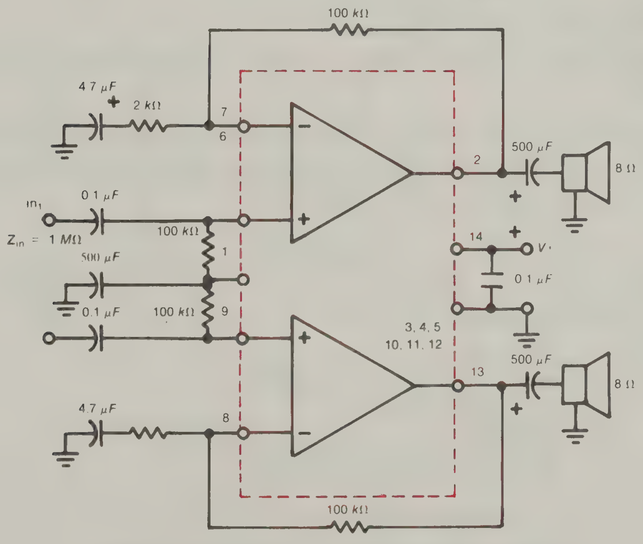

100 kΩ
4.7 μF
2 kΩ
7
6
in₁
0.1 μF
Zᵢₙ = 1 MΩ
100 kΩ
1
500 μF
0.1 μF
100 kΩ
9
2
500 μF
8 Ω
14
V+
0.1 μF
3, 4, 5
10, 11, 12
13
500 μF
8 Ω
4.7 μF
8
100 kΩ

Figure 11-3. LM377 noninverting amplifier
Courtesy National Semiconductor Corporation

The bass portion of the audio signal can be boosted by adding an RC network to the feedback loop, as shown in **Figure 11-4**.

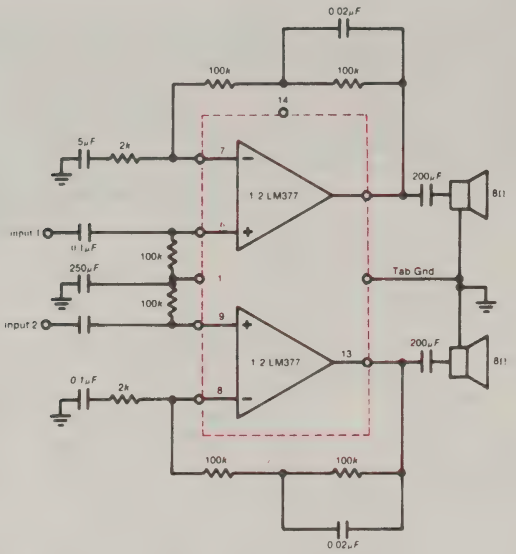

0.02μF
100k
100k
14
5μF
2k
7
1/2 LM377
200μF
8Ω
Input 1
0.1μF
100k
250μF
1
Tab Gnd
100k
Input 2
9
1/2 LM377
13
200μF
8Ω
0.1μF
2k
8
100k
100k
0.02μF

Figure 11-4. LM377 audio amplifier with bass boost
Courtesy National Semiconductor Corporation

For the lower frequencies of the audio band (bass range), the reactance of the capacitor will increase, allowing less feedback and increased gain for those frequencies. The 377 is capable of accepting input signal voltages between 0 volts and V+, but input signal voltages are usually considerably less than 1 volt, to prevent output distortion. The exact peak value of input voltage is a function of the supply voltage and the circuit gain.

Both halves of the 377 may be used in an audio bridge amplifier configuration to drive floating loads, as shown in **Figure 11-5**. In this configuration, twice the output power (4 watts) can be delivered to the load.

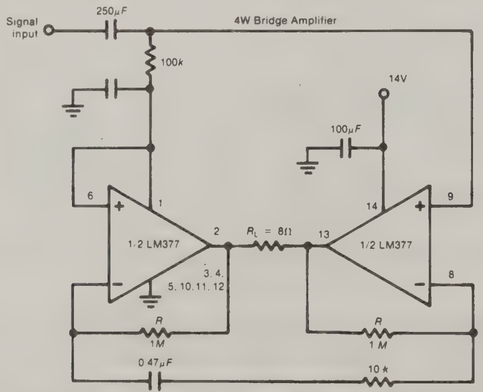

Signal input
250μF
4W Bridge Amplifier
100k
14V
100μF
6
1
14
9
1/2 LM377
2
R_L = 8Ω
13
1/2 LM377
3, 4, 5, 10, 11, 12
8
R
1M
R
1M
0.47μF
10k

Figure 11-5. LM377 4-watt audio bridge amplifier
Courtesy National Semiconductor Corporation

11-3 LM1877 Dual-Power Audio Amplifier

The LM1877 is a pin-for-pin replacement for the 377 dual two-watt audio amplifier. This IC is the manufacturer's recommended replacement for the 377.

The 1877 designation actually covers ten identical devices with unique operating parameters and electrical characteristics (1877N1 through 10). The 1877N1 through 5 share a maximum supply voltage of +20 volts, while the N5 through N10 devices range up to a maximum supply of +26 volts. The most noticeable difference between these devices is the amount of output power they can deliver to a given load value.

With proper selection, the 1877 may be inserted directly into any 377 application. In general, the 1877 offers several improvements over its predecessor. While offering comparable channel separation, ripple rejection, and output power—the 1877 offers a wider choice of supply voltage, lower crossover distortion, and low audio hand noise.

Figure 11-6 depicts the 1877 stereo phonograph amplifier with bass tone control.

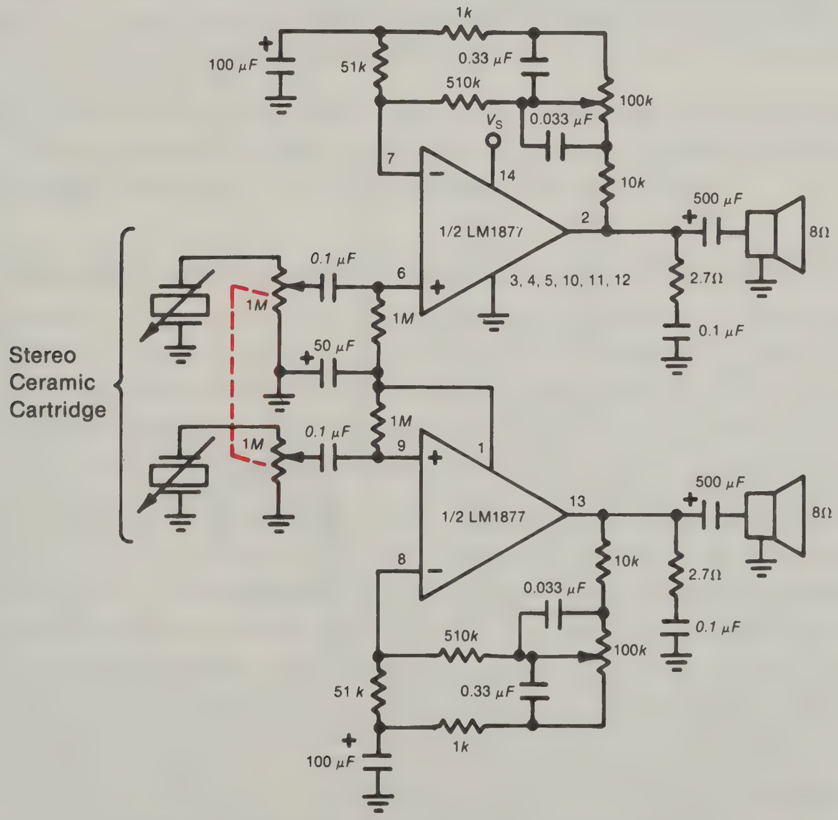

1k
100 μF
51k
0.33 μF
510k
100k
V_S
0.033 μF
7
14
10k
500 μF
2
8Ω
1/2 LM1877
Stereo
Ceramic
Cartridge
0.1 μF
6
1M
3, 4, 5, 10, 11, 12
2.7Ω
0.1 μF
50 μF
1M
9
1
1/2 LM1877
13
500 μF
8Ω
8
10k
2.7Ω
0.033 μF
0.1 μF
510k
100k
51 k
0.33 μF
1k
100 μF

Figure 11-6. LM1877 stereo phono amplifier with bass control
Courtesy National Semiconductor Corporation

This circuit uses a passive bass tone control network in the feedback loop of each amplifier to control low frequency gain. Since human hearing is logarithmic in nature, the potentiometers used in the tone control circuits should also be logarithmic (audio tapered). In other words, a degree of rotation at the upper end of the potentiometer picks off much less resistance than a degree of rotation at the lower end of the pot.

As the potentiometer is adjusted away from the amplifier, the effect of the upper capacitor (in the case of the lower amplifier it would be the lower capacitor) is diminished, while the effect of the lower capacitor is increased and more resistance is added to the feedback loop. This action produces some increased signal gain for all frequencies, but delivers a disproportionate increase in gain for lower frequency (bass) signals.

A similar circuit can be constructed to provide *treble*, or high-frequency tone control. By swapping the components in the bass tone control circuit and reducing the value of the capacitors, as shown in **Figure 11-7**, a passive-treble tone control circuit can be inserted in the amplifiers feedback loop.

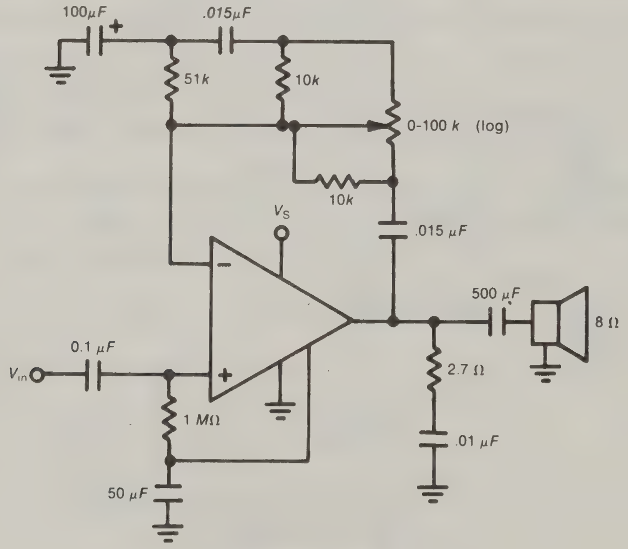


Figure 11-7. LM1877 with treble tone control
Courtesy of National Semiconductor Corporation

These two circuits can also be combined in the feedback loop to provide both bass and treble tone control.

IC manufacturers produce a wide variety of similar audio amplifiers, with various operating characteristics, to fill a wide range of application requirements. The following is a short summarization of some of these devices.

The LM378 is a dual 4-watt audio amplifier which is pin-for-pin compatible with the LM377 and LM1877. It operates with single supply voltages up to 35 volts, and provides many of the same features as the LM377.

The LM379 is a dual 6-watt audio amplifier, which also uses single supply voltages up to 35 volts, and boasts many of the features of the LM377. Unlike the 378, the 379 is not pin-for-pin compatible with the 377, but it can be used in the same applications as the 377.

The LM380 and LM384 are pin-for-pin compatible, 5-watt audio power amplifiers. The 384 is the manufacturer's recommended replacement for the 380.

The LM381 and LM387 are low-noise dual preamplifiers, used to amplify low-level signals in applications where low-noise performance is a must. Both circuits contain two independent, low-noise operational amplifiers, with high gain and single supply operation up to 40 volts.

The LM383 is a single 8-watt audio power amplifier, which can provide large output voltage swings and high peak output currents. The 383 accepts a wide range of single supply voltages (+5 to +20 volts).

11-4 9400 Voltage-to-Frequency/Frequency-to-Voltage Converter

The 9400 is a very flexible IC which can be configured to perform either voltage-to-frequency (V/F) or frequency-to-voltage (F/V) conversion, with a minimum of external components. Actually, the 9400 is one of a series of IC converters (9400, 9401, and 9402) which are pin-for-pin compatible, but differ somewhat in their operational characteristics. The 9400 operates with single (8*V*-15*V*), or dual (+ 4*V*– +7.5*V*) supply voltages, making it easy to interface with any form of digital logic. Care must be taken when working with the 9400, because it is a complementary/symmetry MOS (CMOS) device. These devices are extremely sensitive to static discharge. The static built up on a technician's finger is enough to destroy the chip; therefore, special techniques must be used when handling CMOS ICs. CMOS should never be handled by the technician, unless he is physically grounded to the circuit by a grounding strap. Special insertion tools are available to install or remove CMOS integrated circuits. These ICs should be stored in conductive foam or anti-static storage tubes.

Basically, the 9400 is a voltage-to-frequency converter (VCO), but as is the case with most IC V/F converters, the 9400 may also be configured to perform frequency-to-voltage conversions.

When used as a V/F converter, the 9400 offers temperature stable 1 *Hz* to 100 *kHz* operation, with a guaranteed linearity of 0.05%. The input may be used in the current or voltage driven mode, with input and output scaling provided by external programing resistors. In this mode of operation, the device features two buffered, open collector outputs, which produce pulse and square waves that can be interfaced with virtually any digital logic family.

When used as a frequency-to-voltage converter, the 9400 provides high input impedance (greater than 10 *MΩ*), will accept any input voltage waveshape from DC to 100*kHz*, and features an op amp output. In either mode of operation, the 9400 can be used with single (8 to 15 *V*) or dual (+4 to 7.5*V*) supply voltages, with guaranteed linearity and low power dissipation (27*mW*).

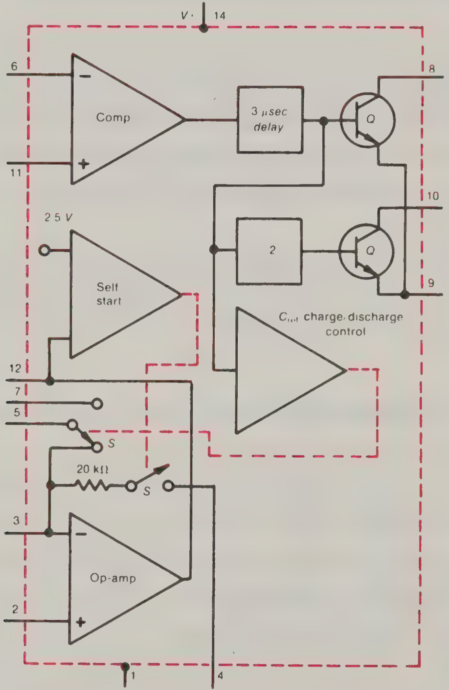


Figure 11-8. 9400 block diagram
Courtesy of Teledyne Corporation

Internally, the 9400 contains many components previously discussed with the VCO of the Norton amplifier chapter, and the VCOs of the phase-locked loop chapter. **Figure 11-8** shows a block diagram of the 9400's internal structure. This device contains: an op amp integrator; an op amp comparator similar to the Schmitt triggers discussed earlier; a 3 microsecond delay circuit; a divide-by-2 counter; a toggle-type flip-flop; two buffered, common ground, open collector output stages; and a charge/ discharge control circuit.

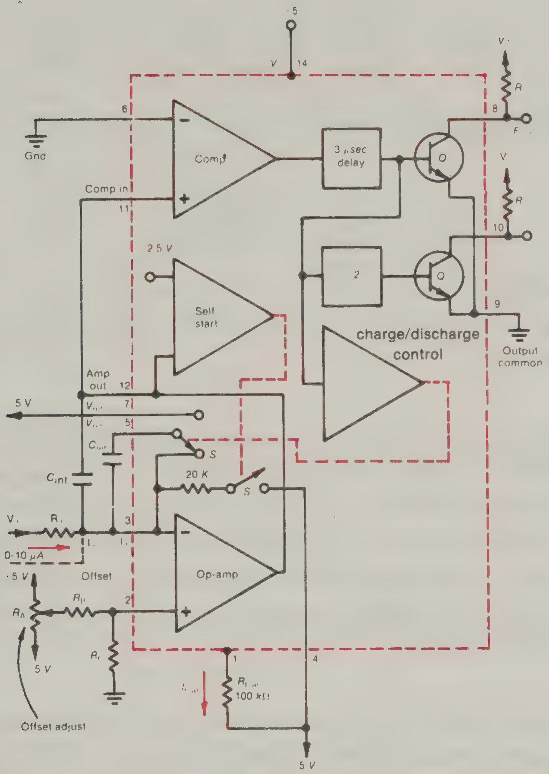

5
V
14
V
R
8
F
V
R
10
9
Output common
Gnd
6
Comp
Comp in
11
3 μsec delay
Q
2
Q
2.5 V
Self start
charge/discharge control
Amp out
12
5 V
7
5
S
20 K
S
C_{int}
V
R
3
0-10 μA
5 V
Offset
Op-amp
R_A
2
5 V
1
4
100 kΩ
Offset adjust
5 V

Figure 11-9. Typical configuration for 9400 voltage-to-frequency converter
Courtesy of Teledyne Corporation

Figure 11-9 depicts a typical connection diagram for a 9400 V/F converter. The op amp integrator is designed to operate with input currents from 0 to 10 microamps. This input can be driven directly with currents in this range, or an input resistance may be used to allow the input to be voltage driven, with I_{in} equal to 10 μA at $V_{in\,(max)}$. The noninverting input may be run to ground or to an external nulling configuration (see Chapter 2). The integrator section makes use of two capacitors: a capacitor for integration and reference capacitor. The relationship between these two components call for C_{int} to be between 3 and 10 times larger than C_{ref}, with optimum performance when C_{int} equals 4 times C_{ref}.

A 100 $k\Omega$ biasing resistor is connected between pins 2 and 4, to supply bias current to the chip. Operation specifications for the 9400 are based on this value of R_{bias}. The V_{ref} pin (pin #7) is usually connected to the negative supply voltage ($V-$), but an external reference voltage may be applied to this pin to alter the input-to-output transfer function. When used in the voltage-to-frequency converter mode, the 9400's output frequency is determined by these factors in the formula:

$$f_{\text{out}} = \frac{V_{\text{in}}}{R_{\text{in}}} \times \frac{1}{V_{\text{ref}}/(C_{\text{ref}})} \tag{11-3}$$

or for current driven operation:

$$f_{\text{out}} = I_{\text{in}} \times \frac{1}{V_{\text{ref}}\,C_{\text{ref}}} \tag{11-4}$$

Notice that C_{in} does not affect the transfer function as long as the relationships stated above are observed.

The output of the integrator (pin 12) is applied to the noninverting input of the op amp comparator (pin 11). The inverting input of the comparator is applied to a reference voltage (ground in this case). The output of the comparator drives the 3 microsecond delay circuit, which in turn drives an open collector output, a divide-by-two flip-flop, and the C_{ref} charge/discharge control amplifier. Notice also that the 9400 contains an internal self-start comparator, which insures automatic V/F operation when power is first applied.

The open-collector output transistors must have external pull-up resistors to operate. The voltages used with these transistors are not limited to the value of the 9400's positive supply, as long as the collector supply is not greater than 18 volts more positive than the 9400's negative supply. The emitters of the output transistors are also open, although they are tied to each other, which allows a great flexibility in output configurations. The f_{out} output (pin 8) produces negative going pulses of approximately 3μ*sec*, while the $f_{\text{out}}/2$ output (pin 10) produces a square wave output.

When power is supplied to the IC, the self-start circuitry insures that the inegratrator output is positive and C_{ref} is discharged. The application of a DC input voltage (or current) will cause the integrator's output to ramp negative in a linear fashion. When the integrator's output ramps below the comparator's reference input (Gnd), the comparator output goes low and drives the output of the 3 μ*sec* delay circuit high after a 3 microsecond delay. This forces the f_{out} output low and causes the C_{ref} charge/discharge control amp to charge C_{ref} to the reference voltage (V_{ref}). This sudden application of negative voltage, at the inverting terminal of the integrator, causes its output to go maximum positive; this in turn causes the comparator output to once again go low. 3 microseconds later, the C_{ref} charge/discharge amp again shorts out C_{ref}, causing it to discharge rapidly. The circuit is now reset and the cycle will be repeated. **Figure 11-10** shows the relative timing waveforms of the 9400.

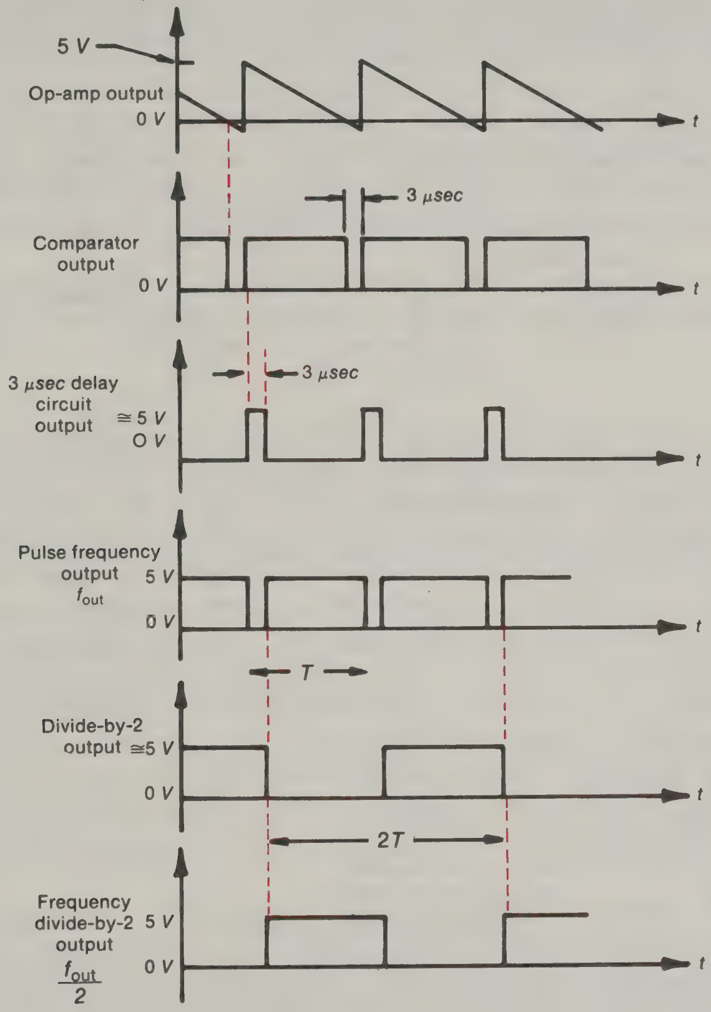

5 V
Op-amp output
0 V
t
3 μsec
Comparator output
0 V
t
3 μsec delay circuit output
≅ 5 V
0 V
3 μsec
t
Pulse frequency output f_{out}
5 V
0 V
t
T
Divide-by-2 output
≅5 V
0 V
t
2T
Frequency divide-by-2 output $\frac{f_{out}}{2}$
5 V
0 V
t

Figure 11-10. Relative timing waveform of 9400 V/F converter

Since the f_{out} output is a common emitter configuration, driven directly from the 3 microsecond delay circuit, the f_{out} output waveform will be in the form of 3 μsec low-going pulses. When the output of the delay circuit is low, the output transistor is cut off and the output voltage level is high. When the delay circuit's output is high, the output transistor is saturated and the output voltage is pulled low.

The $f_{out}/2$ output is driven by a toggle type flip-flop, so two delay pulses are necessary to cause a change of output states.

The 9400 can be used to perform frequency-to-voltage conversions by reconfiguring the external components slightly. **Figure 11-11** depicts the 9400 configured for F/V conversion.

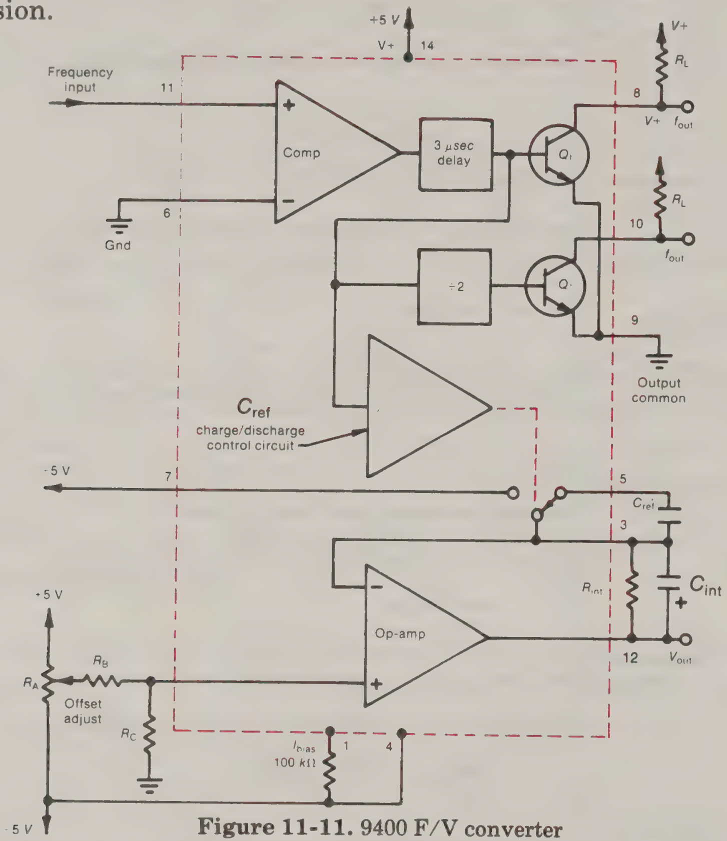

+5 V
V+
14
Frequency input
11
Comp
3 μsec delay
Q_1
8
$V+$
R_L
$V+$
f_{out}
6
Gnd
R_L
10
f_{out}
÷2
Q_2
9
Output common
C_{ref}
charge/discharge control circuit
-5 V
7
5
C_{ref}
3
R_{int}
C_{int}
+5 V
Op-amp
12
V_{out}
R_B
R_A
Offset adjust
R_C
I_{bias}
100 kΩ
1
4
-5 V

Figure 11-11. 9400 F/V converter
Courtesy of Teledyne Corporation

As the figure indicates, the major difference in this mode of operation is the point where the input signal (f_{in}) is applied and from where the output signal (V_{out}) is taken. The frequency input signal is applied to the noninverting input of the op amp comparator stage. The analog output is taken from the integrator output. With input voltages of less than 2 volts, the input signal may be applied directly to the noninverting input. The input signal must have an amplitude greater than $\pm 0.2\ V$ in order to overcome the hysteresis of the comparator. If the input signal is of a single polarity, the comparator should be configured as a positive level detector, with the detection point between the maximum and minimum values of the input signal.

At the integrator output, C_{ref} and C_{int} are configured just as they were with the V/F converter. The values of C_{ref} and C_{int} are fairly standardized for the input frequency range of $f_{in(max)} = 10\ kHz$. At this frequency, C_{ref} should equal approximately $56\ pF$, and C_{int} should be $0.001\ \mu F$. For a higher frequency range, the value of both C_{ref}

and C_{int} may be decreased. A resistor, R_{int}, is also added to the feedback loop of the integrator to scale the analog output voltage. To scale the output for a maximum input frequency of 100 *kHz*, R_{int} should be 100 *k*Ω; and to scale the output for a maximum input frequency of 10 *kHz*, the value of R_{int} should be increased to 1 *M*Ω. The value of R_{int} should be made variable to allow easy calibration of the output voltage. Digital outputs are also available when using the F/V mode. (The f_{out} output produces a waveform which allows the input frequency with a 3 microsecond delay).

The $f_{out}/2$ output produces a square-wave at ½ the frequency of the input signal. The analog output voltage of the 9400F/V converter is calculated by the formula:

$$V_{out} = (R_{int}\ C_{ref}\ V_{ref})\ f_{in} \tag{11-5}$$

The output of the comparator goes low each time the input signal drops below the reference voltage on its inverting terminal. Three microseconds later, the C_{ref} charge/discharge amp begins charging C_{ref} to the 9400's reference voltage (V_{ref}).

The integrating capacitor (C_{int}) is also charged during this time, to a value proportional to the width of the input's low time (Typical integrator action).

When the input signal is more positive than the comparator's reference voltage, its output goes high, causing the C_{ref} charge/discharge amp to discharge C_{ref}. C_{int} also discharges through R_{int} at this time. Since the value of R_{int} is relatively large, C_{int} will not be allowed to discharge very rapidly. As the input frequency increases, the integrating capacitor continues to charge toward V_{ref} through C_{ref}, but will not be able to discharge as far, due to the shortened discharge time. Therefore, as the input frequency increases, so does the level of the output voltage. For proper operation, the duty factor of the input signal should be greater than 20%, with both t_1 and t_2 greater than 0.5 μsec.

When designing the 9400 for F/V or V/F operation, several design steps are common to both modes. First, an appropriate set of supply voltages (single or dual), and a reference voltage must be chosen. V_{ref} is usually chosen to equal the lower supply voltage, but may be established by a separate source. Next, make R_{bias} equal to 100 *k*Ω and choose suitable values of f_{out}, $f_{out}/2$ and output pull-up resistors, such as 10 *k*Ω. If these outputs are not used in F/V conversions, pins 8, 9, and 10 may be tied to ground. Lastly, an offset null circuit should be constructed at pin 2, with R_A greater than R_C, and R_B greater than R_A.

The input may be current or voltage driven ($I_{in\,(max)} = 10\ \mu A$). If the input is to be voltage driven, the input must be scaled by an input resistor (R_{in}). The value of R_{in} is calculated by the formula:

$$R_{in} = \frac{V_{in}\,(\text{max})}{10\ \mu A} \tag{11-6}$$

R_{in} may be made adjustable to allow easy output range calibration.

The value of C_{ref} is calculated from the formula:

$$C_{ref} = \frac{V_{in(max)}}{(V_{ref})(R_{in})f_{out(max)}} \tag{11-7}$$

or:

$$C_{ref} = \frac{10\ \mu A}{(V_{ref})f_{out(max)}} \tag{11-8}$$

C_{ref} should be less than 500 *pF* and C_{int} should be as close to 4 times C_{ref} as possible. High-quality capacitors should be used for accuracy, and they should be physically located as close to the IC as possible.

The value of R_{int} should either be chosen at the standard values stated earlier ($R_{int} = 100\ k\Omega$ for $f_{in(max)} = 100\ kHz$ or $1\ M\Omega$ for $f_{in(max)} = 10\ kHz$), or made adjustable across these ranges to allow for easy V_{out} range calibration. C_{ref} and C_{int} should be chosen to be approximately 47 *pF* and 100 *pF* respectively, for an input frequency range of 10 *kHz*. The value of both capacitors may be decreased for lower input frequency ranges.

Both modes of operation may be configured to allow for exact input to output calibration. The offset null circuitry is used to *zero* both modes of operation. With the minimum input signal applied to the circuit ($f_{in(min)}$ for F/V conversion and $V_{in(min)}$ for V/F conversion), the offset null circuitry is adjusted until the minimum output level is established. With the input level set at the maximum, R_{int} is adjusted until the maximum output voltage is achieved for the F/V converter, or R_{in} is adjusted until the maximum output frequency is achieved for the V/F converter. These steps may need to be repeated to insure proper zeroing and span (range).

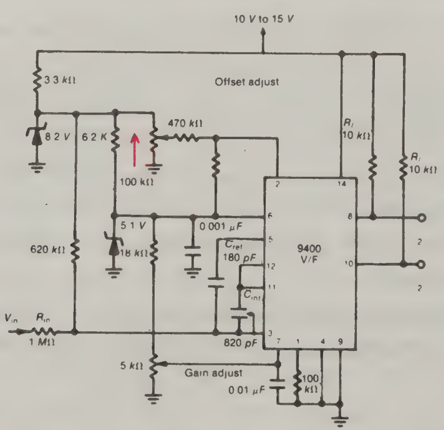


Figure 11-12. Single supply 9400 V/F converter.
Courtesy of Teledyne Corporation

Single supply operations with the 9400 require special input and/or output considerations. **Figure 11-12** depicts a 9400 V/F converter, configured for single supply operation. The offset null and the comparator's reference (−) input are referenced above ground by reverse-biased zener diodes.

When the 9400 F/V converter is used with a single supply, both the comparator's input and the 9400's output are referenced to a preset level, as shown in **Figure 11-13**.

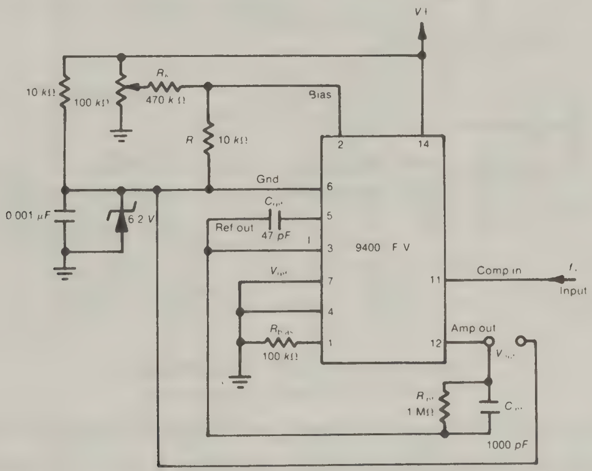


Figure 11-13. Single supply 9400 F/V converter
Courtesy of Teledyne Corporation

The 9400 may be adapted to perform in a variety of applications. In many applications, two 9400s are used, one in each mode, to convert an analog voltage signal into a more easily transmitted frequency signal, and the other to convert the frequency signal back to an analog signal after transmission. The 9400 V/F converter configuration is often used to convert an analog voltage signal into a digital frequency or pulse waveform signal, for transmission over telephone lines or by an FM transmitter. When transmitting data over long distances, digital signals are generally the preferred method of transmission. Digital signals are less susceptible to noise than other forms of transmission. Square-wave digital signals are more common than pulse waveforms, due to the excessive portion of the frequency spectrum necessary for pulse waveform data transmission.

At the receiving end of the transmission, the 9400 F/V converter can be used to convert the digital signal back into an analog signal or to demodulate the FM signal.

Matching 9400s are also excellent in frequency-shift-keying (FSK) generation and decoding systems. Dual inputs are used with a 9400 V/F converter to establish the logic "0" and logic "1" output frequencies, as shown in **Figure 11-14**. The lower output frequency, which corresponds to a logic 0 or low input voltage, is set by the reference potentiometer and $R_{\text{in(low)}}$. When a digital 1 logic voltage is applied to the input, current will be added to the reference current, causing the output frequency to shift to the upper (logic 1) output frequency.

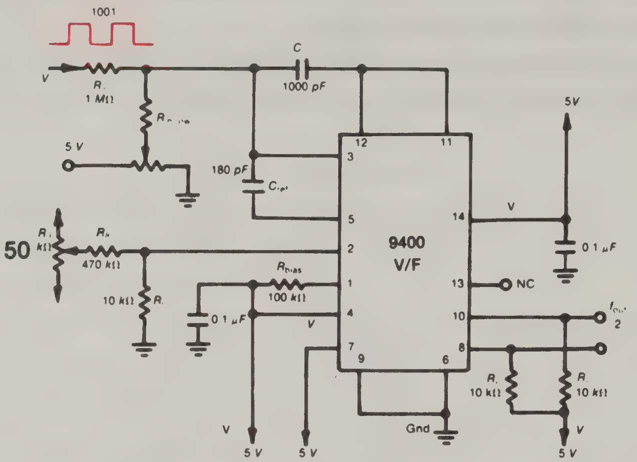

1001
C
1000 pF
V
R.
1 MΩ
R
5 V
180 pF
C
5V
12
11
3
5
14
V
9400
V/F
2
1
13
4
10
7
9
6
8
0 1 µF
NC
f
2
50
R
kΩ
R
470 kΩ
R bias
100 kΩ
10 kΩ
R.
0 1 µF
V
R.
10 kΩ
R.
10 kΩ
V
Gnd
V
5 V
5 V
5 V

Figure 11-14. 9400 FSK generator.
Courtesy of Teledyne Corporation

The 9400 FSK generator may be designed using single or dual supply voltages for most digital logic families. **Figure 11-15** lists a set of standard FSK operating frequencies.

0	1
1070 *Hz*	1270 *Hz*
2125 *Hz*	2975 *Hz*
2025 *Hz*	2225 *Hz*

Figure 11-15. Standard FSK fequencies

As an example, the TTL logic family produces logic 1's of approximately +5V and logic 0s of approximately 0 volts. If TTL data is to be transmitted using the 2225/2075 *Hz* FSK relationship, the V/F converter should be designed using the steps mentioned earlier. The exception is that $R_{\text{in(low)}}$ should be calculated to produce an output frequency of 2075 *Hz* using a preset value of potentiometer voltage. This step is accomplished by rearranging the V/F output formula:

$$f_{\text{out}} = \frac{V_{\text{in}}}{R_{\text{in}} V_{\text{ref}} C_{\text{ref}}} \tag{11-9}$$

$$R_{\text{in(low)}} = \frac{V_{\text{pot}}}{f_{\text{out(low)}} V_{\text{ref}} C_{\text{ref}}} \tag{11-10}$$

The value of $R_{\text{in(high)}}$ can be calculated by expanding the formula to include both inputs and the value of TTL logic 1 voltage.

$$f_{\text{out(high)}} = \left(\frac{V_{\text{adj}}}{R_{\text{in(low)}}} + \frac{V_{\text{TTL}}}{R_{\text{in(high)}}}\right)\frac{1}{V_{\text{ref}}C_{\text{ref}}} \qquad (11\text{-}11)$$

$$f_{\text{out}} = \frac{V_{\text{adj}} + V_{\text{TTL}}}{(R_{\text{in(low)}} + R_{\text{in(high)}})V_{\text{ref}}C_{\text{ref}}} \qquad (11\text{-}12)$$

$$R_{\text{in(low)}} + R_{\text{in(high)}} = \frac{V_{\text{adj}} + V_{\text{TTL}}}{f_{\text{out(high)}}V_{\text{ref}}C_{\text{ref}}} - R_{\text{in(low)}} \qquad (11\text{-}13)$$

TTL logic levels are not exactly 0 and 5 volts, so the generator will need to be calibrated using the steps outlined earlier. It is important to remember that the sum of the two input currents must be less than 10 μA.

At the receiving end, a 9400 F/V converter and a simple op amp level detector can be combined to demodulate the FSK signal, as shown in **Figure 11-16**.

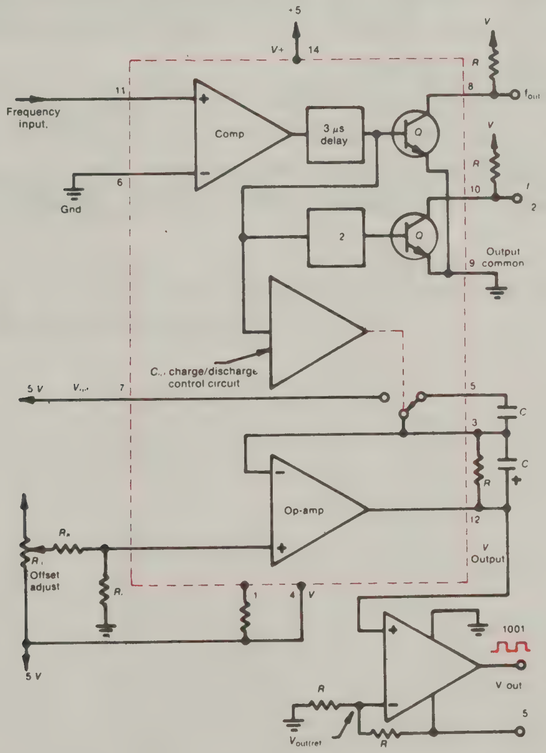

+5
V+
14
V
R
8
f_out
Frequency input.
11
Comp
3 µs delay
Q
V
R
10
1/2
6
Gnd
2
Q
Output common
9
C... charge/discharge control circuit
5 V
V...
7
5
C
3
C
R
Op-amp
12
R_x
R
Offset adjust
R.
V Output
1
4
V
1001
V out
5
R
R
V_outref
5 V

Figure 11-16. 9400 FSK demodulator
Courtesy of Teledyne Corporation

As the FSK input signal shifts from one logic frequency to the other, the 9400's analog output voltage also shifts between two preset voltages. These output voltages are applied to the level detector, which operates with a TTL compatible 0 to +5 volt supply. The comparator's reference voltage is established so that the lower 9400 output voltage produces a low (0) output and the upper 9400 voltage produces a high (+5) output level.

The 9400 demodulator is designed in exactly the same manner as the simple F/V converter discussed earlier.

The value of V_{ref}, C_{ref}, or R_{int} can be adjusted to provide the desired output voltage levels. The comparator's reference (inverting input) voltage is chosen to be half way between $V_{out(low)}$ and $V_{out(high)}$.

RF modulation and demodulation is accomplished with the 9400 in much the same way as FSK generating and decoding. A 9400 RF modulator is configured the same as the FSK generator, as shown in **Figure 11-14**. The only differences between the two are that the potentiometer is set to produce the RF carrier (center) frequency, and the input signal is an analog rather than a digital signal. The 9400 V/F converter makes a very linear FM modulator, which can accept both positive and negative input voltage swings.

The 9400 V/F converter is also widely used in applications such as phase-locked loops, digital meters and analog-to-digital (A/D) converters. The 9400 used in the F/V mode can be found in applications such as frequency meters, tachometers, FM/FSK demodulators, and frequency/tone detector/decoders.

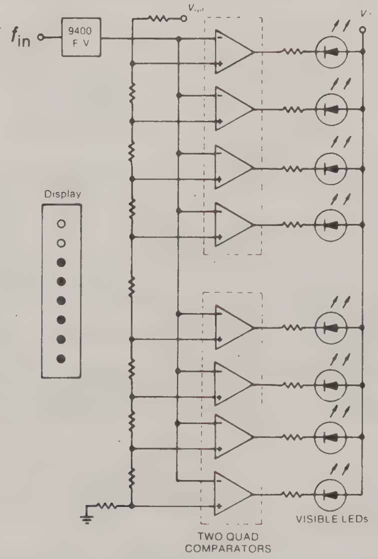


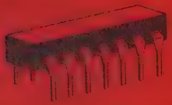
Figure 11-17. Tachometer bar graph display
Courtesy of Teledyne Corporation

Figure 11-17 depicts a 9400 F/V converter, used to drive an op amp multi-level detector, which in turn drives a bar of LEDs. This type of arrangement can be used to produce a bar-graph tachometer, with the number of lighted LEDs being proportional to revolutions per minute (RPM).

11-5 Summary Points.

1. The LM377 is a simple dual op amp package used primarily as a stereo amplifier with 90*dB* of open-loop gain and 75*dB* of channel separation.
2. The LM1877 is a direct replacement device for the LM377 and comes in ten variations. The biggest difference between each variation is power handling capability.
3. The 9400 IC can be configured as a voltage-to-frequency or frequency-to-voltage converter with a minimum of external components.
4. CMOS ICs are extremely sensitive to static discharge and special handling techniques must be utilized.
5. The 9400 IC is widely used in PLL digital meter circuits, and analog-to-digital converters, in the V/F mode.
6. When configured in the F/V mode, the 9400 is found in frequency meters, tachometers, FM/FSK demodulators, etc..

Chapter 12



Glossary

Absolute maximum ratings: Electrical limitations set by manufacturers which must not be exceeded.

Active elements: Transistors and op amps.

Active filters: Filter circuits which employ active elements.

Adder: See summing amplifier.

Adjustable voltage regulator: A regulator circuit in which a few external components are added to a fixed regulator to provide adjustable levels of regulated output voltage.

Alphanumeric code: A code composed of letters and numbers used by manufacturers to identify their products.

Ambient temperature: The temperature of the air around a circuit or component.

Analog signal: A signal that varies smoothly or continuously with no abrupt changes.

Astable: No steady state.

Astable multivibrator: A self-starting, free-running square or rectangle wave generator whose frequency is determined by the value of external components.

Attenuation: A reduction of signal amplitude due to a circuit or device.

Averaging amplifier: A type of summing amplifier where the feedback resistor is chosen to produce an output that is the average of a set of input signals.

Bandpass: A filter which passes a group of frequencies within the frequency spectrum while attenuating the extreme high and low frequencies of the spectrum.

Band-reject filter (notch filter): A filter which passes the extreme high and low frequencies of the spectrum while attenuating a group of frequencies within the frequency spectrum.

Bandwidth: The difference between the upper and lower cutoff frequencies of a filter network.

Barkhausen Criterion: A statement of the conditions necessary for an oscillator to be self starting and self perpetuating. The product of the amplifier gain and the fractional feedback factor must be equal to one.

Beta (β): The ratio of a transistor's collector current to its base current.

Breakpoint: See cutoff frequency.

Buffer: A circuit used to isolate one circuit from another.

Butterworth response: A filter response which produces a flat response amplitude within the passband of the filter.

Capture mode: A PLL mode which occurs when an error voltage causes the VCO output frequency to change.

Capture range: The range of frequencies over which capture is possible.

Cascading: The practice of connecting the output of a filter or amplifier to the input of the next stage to enhance the operating characteristics of the circuit.

Center frequency (f_r): The frequency at which the response curve reaches maximum amplitude.

Chip: A small piece of semiconductor material on which an integrated circuit is formed.

Common-base amplifier: A low input impedance, high output impedance, noninverting amplifier configuration. The input is applied to the emitter and the output is taken from the collector.

Common-emitter amplifier: A high input impedance, low output impedance, inverting amplifier configuration. The input is applied to the base, and output is taken from the collector.

Common-mode biasing: A method of biasing Norton amplifiers to allow voltages less than V_{BE} to be used.

Common-mode rejection ratio: The ratio comparison of a differential amplifier's ability to amplify a differential input signal while rejecting a common-mode input signal.

Common-mode signal: One of two identical phase and amplitude signals applied to both inputs of a differential amplifier.

Comparator: An open loop op amp circuit which compares a signal voltage to some reference voltage level or another signal voltage. The output of these types of circuits is used only to indicate the relative values of the two voltages.

Compensation: Use of external components to stabilize ICs.

Complementary-symmetry amplifier: A unity voltage gain, low output impedance configuration widely used as an IC output stage. Two output transistors divide the output signal with one transistor conducting on the positive half cycle and the other transistor conducting on the negative half cycle.

Constant-current regulator: Variation of a fixed three-terminal regulator circuit which provides a constant output current.

Constant-current source: Circuit which provides a constant level of output current over a varying range of load conditions.

Constant-voltage reference: Circuit or device used to provide a constant level of voltage over a varying range of load conditions.

Control voltage: An external voltage used to modify the timing relationship of a timer circuit. Used to alter both the threshold and trigger levels.

Crystal oscillator: Oscillator circuit which uses the stability of a crystal's natural frequency of vibration to provide a highly stable oscillator.

Current differencing amplifier: Norton Amplifier. Type of amplifier which responds to an input current differential rather than an input voltage differential.

Current limiter: Series-pass transistor configuration used to provide over current protection.

Current mirror: Any circuit in which the output current is forced to equal the input current. Input stage of a Norton amp.

Cutoff frequency (f_c) The frequency at which the output voltage of a filter drops off to 70.7% of its maximum value.

Damped natural frequency: The frequency at which the PLL will oscillate in the presence of damping with no input signal applied.

Damping: The determining factor in the shaping of a filter's response curve, represented by the Greek letter alpha (α).

Darlington pair: Two transistor emitter-follower circuits used to provide high current gain and increased signal sensitivity.

Differentiator: A circuit which produces an output that is proportional to the rate of change of the input signal.

Differential input resistance: Op amp's input resistance under open loop conditions.

Decade: A tenfold increase or decrease in frequency from f_c.

Decibel: Unit used to express an increase or decrease in gain of a circuit.

Degenerative feedback: Feedback out-of-phase with the input signal so that it subtracts from the input.

Difference amplifier: Circuit which produces an output which is the difference of two input signals.

Diffusion: Forcing or driving impurities to the desired depth in silicon wafers to establish desired electrical characteristics.

Digital signal: Signals which change in discrete steps with short transition periods.

Discharge: Terminal used to discharge the timing capacitor in IC timer circuits.

Discrete components: Components which are not physically contained within an IC.

Dissipative voltage regulator: Regulator which uses an active element as a variable resistance to obtain output regulation.

Dopant: Positively or negatively charged impurity deposited onto wafer surface to establish P and N type structures.

Drift: Change in offset voltage and current due to change in temperature, supply voltage, or time.

Drop-out voltage: Minimum voltage which can be applied to a three terminal regulator while maintaining a regulated output. Typically V_{out} regulated plus two volts.

Dual: Two identical circuits in a single package.

Dual-in-line package (DIP): Convenient type of IC packaging in which IC connections are brought through the sides of the package and bent downward in two parallel rows allowing easy chip mounting.

Dual-tracking regulator: Voltage regulator circuit which provides both positive and negative regulated voltages which track (follow) each other.

Dual (split) power supply: A power source which provides equal positive and negative voltages.

Duty cycle: The ratio of the "up" time of a signal to the total period of the signal expressed in percent. Also referred to as *duty factor.*

Equal component filters: Second-order filters where all frequency determining resistors and capacitors are made equal and gain is held at approximately 1.5.

Emitter-follower: Unity voltage gain amplifier configuration with high input impedance and low output impedance where the signal is applied to the base of a transistor and the output is taken from the emitter. Common-collector amplifier. Isolation amplifier.

Etching: Process of creating windows in the surface of the silicon wafer.

Extended astable operation: A stable timer configuration which provides duty cycles of less than 50%.

External nulling: Resistor network used to compensate DC offset voltage in an op amp.

Feedback: Practice of applying a portion of a circuit's output signal back to its input.

Feedback element: Resistor or capacitor connected between the input and the output of a circuit to control the amount of feedback signal.

FET: Field-effect transistor.

Filter: A frequency sensitive circuit which is designed to separate groups of frequencies by passing a desired group of frequencies and blocking all the other frequencies.

Fixed voltage regulator: Simple three terminal IC device which provides a fixed, regulated output voltage with no external components required.

Flat-pack: IC packaging where the external terminals extend from the side of the package. A low-profile space saving package signals.

Flip-flop: Digital output device whose output is determined by the sequence of a set of input signals.

Floating load: An ungrounded load.

Free-running mode: PLL mode where no input frequency is close enough to the VCO frequency to be captured.

Frequency compensation: Internal or external capacitor network used to prevent undesired oscillations.

Frequency shift keying: Method of varying the carrier of frequency rather than keying a transmitter on and off.

Frequency synthesis: PLL application in which two frequencies are mixed to produce a desired output.

Frequency-to-voltage converter: A circuit which converts an input frequency signal to a corresponding analog output voltage.

Function generator: Any circuit which produces two or more output waveforms.

Gain bandwidth product (GBP): The product of the gain and bandwidth which is always equal to the unity gain frequency. Useful in finding bandwidth for a given gain.

Gain, closed loop: Ratio of the output voltage to a differential input voltage with degenerative feedback applied.

Gain, differential: Ratio of the output voltage to a differential input voltage.

Gain, open loop: Ratio of the output voltage to a differential input voltage with no feedback applied.

Half-power point: Cutoff frequency of a filter.

Heat sink: A device used to transfer heat away from ICs or components.

High-pass: Filter which passes frequencies above f_c and attenuates frequencies below f_c.

Hybrid IC: Combination of monolithic and thick or thin film devices in a single package.

Hysteresis: A lagging behind. A situation which produces different values for a given point depending on the direction of approach.

Hysteresis voltage: Difference between upper and lower trip point voltages in a Schmitt trigger.

Input bias current: The average of the two input currents in an op amp with no signal applied.

Input element: Passive device between the input signal and the input terminal of an IC.

Input impedance: Usually specified as input resistance.

Input offset current: Difference between the two input bias currents of an op amp

Input offset voltage: Absolute value of voltage that must be applied to the inputs of an op amp to force the output to zero with no input signal present.

Input resistance: The resistance measured from either input of an op amp the with other grounded.

Input voltage range: The range of voltages (common mode) that can be applied to the inputs over which the op amp is linear.

Instrumentation amplifier: Extremely high input impedance difference amplifier configuration.

Integrated circuit: A complete electronic circuit constructed on a tiny piece of semiconductor material. A chip.

Integrator: A circuit whose output represents the magnitude of an input signal and the amount of time the input has been applied. Also used as a wave shaping circuit.

Internal nulling: Op amps which provide external nulling or balance terminals to allow correction of output offset voltage.

Internal power dissipation: The power consumed by an IC with no load and no input signal.

Inverter: Digital device which changes an input logic level (high/low) to the opposite logic level (low/high).

Inverting amplifier: An op amp configuration which produces an output which is 180 ° out-of-phase or the opposite polarity of the input signal.

Isolation amplifier: Amplifier circuit used to provide electrical isolation between stages.

JAN part number: Joint Army-Navy numbering system used by manufacturers who provide ICs for military applications.

Latch up: Condition which occurs mostly in older styles of op amps where the output voltage remains in saturation, after the input which caused the condition has been removed.

Lead-lag filter: A filter that distinguishes between a leading and lagging input signal.

Level detector: Open-loop op amp circuit which compares an input signal voltage to a reference voltage level and produces an output which indicates the relative polarity of the input signal to the reference.

Linear IC: Integrated circuits specifically designed to process analog signals.

Linear signal: An analog signal.

Line regulation: The measure of a regulator's ability to maintain a constant output level under varying supply conditions.

Load protection: Power supply regulator circuitry which limits output voltage or current.

Load regulation: The measure of a regulator's ability to maintain a constant output level under varying load conditions.

Lock mode: PLL mode where the loop's output frequency matches the input frequency.

Lock range: The range of frequencies over which a PLL is capable of tracking an input signal once lock has occurred.

Lower frequency: The lower cutoff frequency of a bandpass or notch filter.

Low-pass: A filter which passes all frequencies below cutoff and attenuates all frequencies above cutoff.

Masking: A series of operations used to selectively produce windows in the epitaxial layer of an IC wafer.

Metal-cannister package: A type of IC packaging where the chip is enclosed in a metal shield and leads are brought out from the base of the package similar to transistors.

Monolithic fabrication: Process which produces high quality integrated circuits on a single substrate.

Monostable: Having a single steady state.

Monostable multivibrator: A one-shot. Produces a single output pulse of fixed duration when triggered.

Multiple feedback: A filter with more than one feedback path for increased filter action. Must have a circuit gain of "one" to produce a Butterworth response.

Multivibrator: Circuit which produces square or rectangular output wave forms.

Narrow bandpass: A highly selective bandpass filter whose bandwidth is less than 10% of the value of the center frequency (f_r).

Natural frequency: The frequency at which a PLL will operate in the free-running mode with no damping.

Natural frequency of vibration: The operating frequency of a crystal.

Noninverting amplifier: An amplifier which produces an output signal which is in-phase with its input signal.

Norton amplifier: Current differencing AC amplifier. Designed to operate with a single supply voltage; locks the high performance characteristics of conventional op amps.

Notch filter (Band-reject filter): A filter which passes the extreme high and low frequencies of the spectrum while attenuating a group of frequencies within the frequency spectrum.

Null frequency: The center frequency of a twin-T filter. At this frequency no current passes through either T.

Offset null: Adjusting the quiescent output voltage of an op amp to zero.

One shot: Monostable multivibrator.

Operational amplifier (op amp): A high gain, DC differential amplifier.

Optoisolator: An electrical isolation device which contains a photo detector and an infrared LED.

Order: A description of the rolloff rate of a filter. The higher the filter's order, the faster the output rolls off.

Oscillator: A circuit which generates an AC pulsating DC output from a DC input.

Output impedance: Resistance of an op amp measured from its output terminal to ground in an open loop configuration.

Output offset voltage: Quiescent output voltage of an op amp without nulling.

Output short-circuit current: The output current when the output is connected directly to ground or a supply voltage.

Output voltage swing: The maximum output voltage which can be obtained without signal clipping.

Over voltage protection: Zener diode configuration used to prevent the application of over voltage to an op amp's power supply terminals.

Overshoot: An output voltage swing, in excess of its final value, in response to a rapid input voltage change.

Oxidation: IC fabrication step where a thin layer of oxide is produced on the surface of a silicon wafer.

Packaging: Material surrounding an IC which protects the circuit, dissipates the heat and gives the circuit usable form.

Passband: The group of frequencies which pass through a filter virtually unaffected.

Passive filter: A filter which uses no active elements. RC, RL or RCL filters.

Phase detector: A comparator circuit which compares two input signals and produces an average DC voltage proportional to the phase difference of the inputs.

Phase difference: The time between two related events expressed in radians or degrees.

Phase-locked loop (PLL): A feedback loop system which locks onto an input frequency signal and tracks (follows) any change in that input frequency.

Phase-lock mode: See lock mode.

Pierce oscillator: A crystal controlled oscillator circuit where the crystal acts as an inductance in parallel with a capacitor network.

Power supply current: The current a circuit draws from a power supply under quiescent conditions.

Power supply rejection ratio: The ratio of a change of supply voltage to the resulting change of input offset voltage.

Pro-electron: A standardized numbering system for integrated circuits.

Pulse width: Time duration of a pulse.

Pulse-width modulator: A circuit which produces an output pulse with a duration which is proportional to an applied error voltage.

Quad: Four identical circuits in a single package.

Quadrature oscillator: A sine/cosine oscillator. Circuit which produces two sinewave outputs 90° out-of-phase.

Quality: The ratio of the center frequency of a bandpass or notch filter to its bandwidth.

Quiescence: A rest or inactive state where no input signal is applied.

Reference voltage: A voltage level applied to one input to use for comparison.

Regenerative feedback: Feedback in-phase or positive feedback which adds to an input signal and tends to create an oscillator.

Reset: Timer input terminal which allows the operator to force its output to the low state.

Response time: The time between the application of an input signal and the output reaching its final value.

Ripple rejection: The ability of a regulator circuit to reject variations in supply voltage.

Rise time: The time required for an output to change from some previous level to within 10% of its final value.

Rolloff: The rate at which a filter attenuates a signal as frequency varies from cutoff.

Saturation: The maximum positive or negative voltage level which an output can obtain.

Scaling amplifier: Variation of the summing amplifier where the inputs have different values of input resistance and allow different inputs to have more or less influence on the output than others.

Schmitt trigger: A bistable trigger circuit that converts an AC input signal into a square wave output signal by switching action, triggered at a predetermined point in each positive and negative swing of the input signal.

Scribing: Cutting the silicon wafer into the hundreds of individual IC chips.

Selectivity: The ability of a bandpass filter to pass a desired frequency while rejecting all other frequencies.

Sensing element: A transistor or op amp used to compare the output voltage to a reference voltage in a series pass voltage regulator. This element drives the series pass (control) transistor.

Series-pass transistor: A variable resistance control element placed in series with the load.

Series regulator: Regulator circuit which places the variable control element in series with the load.

Settling time: The time between the initiation of an input signal change and the time at which the output settles within 10% of its final value.

Shunt regulator: Regulator where the control element is placed in parallel with the load.

Sine/cosine oscillator: See quadrature oscillator.

Single voltage supply: A power supply which provides only a single positive or negative voltage.

Slew rate (SR): The maximum rate of change of an op amp's output.

State variable: A multiple feedback filter circuit which delivers three types of filtering simultaneously.

Stopband: The group(s) of frequencies which a filter attenuates.

Strain gage: A transducer which converts a physical change of shape to a change of resistance.

Substrate: The silicon base upon which ICs are constructed.

Subtractor: A difference amplifier with a gain of one.

Summing amplifier: An amplifier whose output is the sum of a set of input voltages.

Summing point: The junction of the input with the feedback network in an operational amplifier circuit.

Switching regulator: A regulator circuit where the control element is used as an on/off switch resulting in a highly efficient circuit.

Temperature coefficient: The change of voltage or resistance of a circuit or device with a change in temperature.

Thermal overload: A condition of excessive operating temperature.

Thermal shut down: A form of circuit protection where the output of an IC is disabled by excessive temperature.

Thermocouple: Two dissimilar metals joined to produce a small voltage, which is a function of the temperature present at the junction of the two metals.

Thick film: A method of producing passive ICs by a silk screen process.

Thin film: A method of producing passive ICs by repeatedly depositing metal oxide films.

Threshold: IC timer terminal which determines the output state of the timer.

Tracking mode: See lock mode.

Transducer: A device which converts a signal from one form to another.

Transient response: The output response to a change in input signal.

Transistor-transistor logic (TTL): The most popular digital IC logic family.

Twin-T: A passive phase shifting configuration used in both active bandpass and notch filters.

Unity gain bandwidth: The bandwidth when an op amp's gain is reduced to one.

Unity gain frequency: The frequency at which the op amp's gain is reduced to one.

Always equal to the gain-bandwidth product.

Upper frequency: The upper frequency of a bandpass or notch filter where the response is equal to 70.7% of the maximum response.

Varactor: A device which uses the inherent capacitance of a semiconductor diode as a variable capacitance.

Virtual ground: Any point in a circuit which operates at the same potential as ground, but is physically separated from ground.

Voltage controlled oscillator: Oscillator circuit in which the output frequency is determined by the level of the DC input voltage.

Voltage follower: An amplifier with a gain of one where the output follows the input signal. May be inverting or noninverting (buffer).

Voltage level detector: A comparator circuit which has a DC reference voltage applied to one input and an input signal applied to the other.

Voltage-to-frequency converter: See VCO.

Wafer: The semiconductor material on which a batch of identical circuits are formed.

Wide bandpass: A bandpass filter where the bandwidth is greater than 10% of the center frequency.

Wien-bridge oscillator: Oscillator circuit which uses both degenerative and regenerative feedback whose output frequency is determined by an RC frequency selective network.

Window detector: Op amp comparator circuit designed to monitor an input signal and indicate when the signal is either operating within preset limits or exceeds those limits.

Zero crossing detector: A comparator circuit with one input grounded as the reference.

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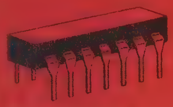

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